可编程逻辑：PLD/FPGA

硬禾实战营培训

内容

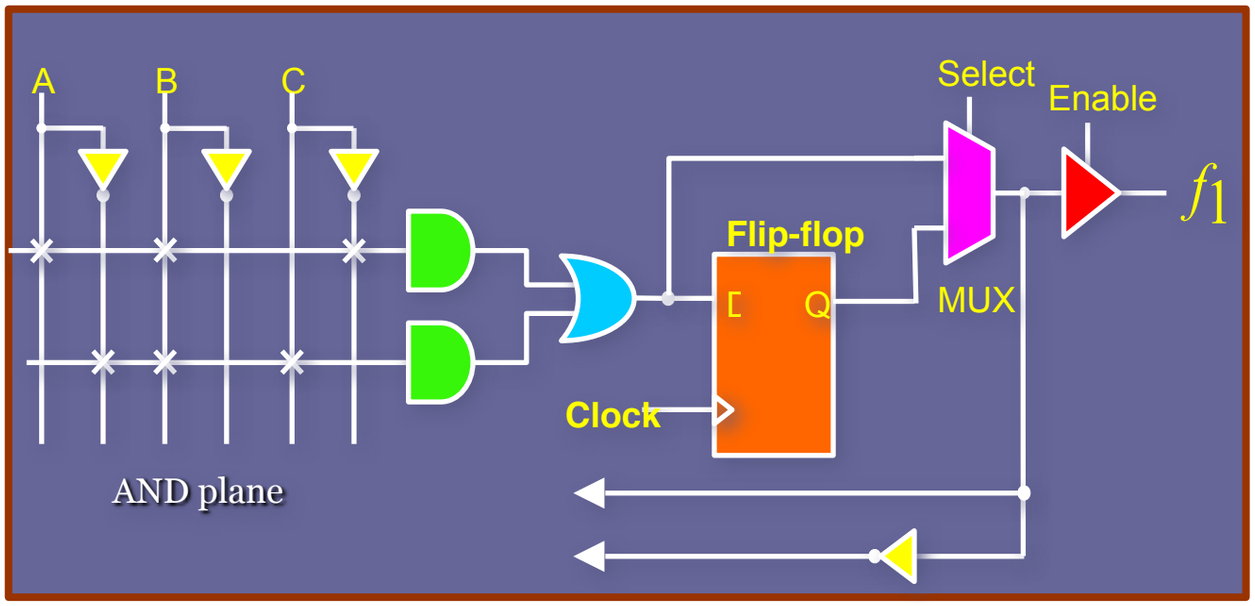
- 为什么用PLD/FPGA?
- PLD/FPGA的结构
- 主要供应商
- FPGA的选型原则
- FPGA的设计流程及设计工具
- FPGA的系统应用
  - 硬件设计
  - 代码开发
- FPGA的资源
  - 开发板
  - IP cores

为什么用可编程逻辑?

FPGA – 设计者可以在现场对可定制的数字逻辑进行编程的集成电路

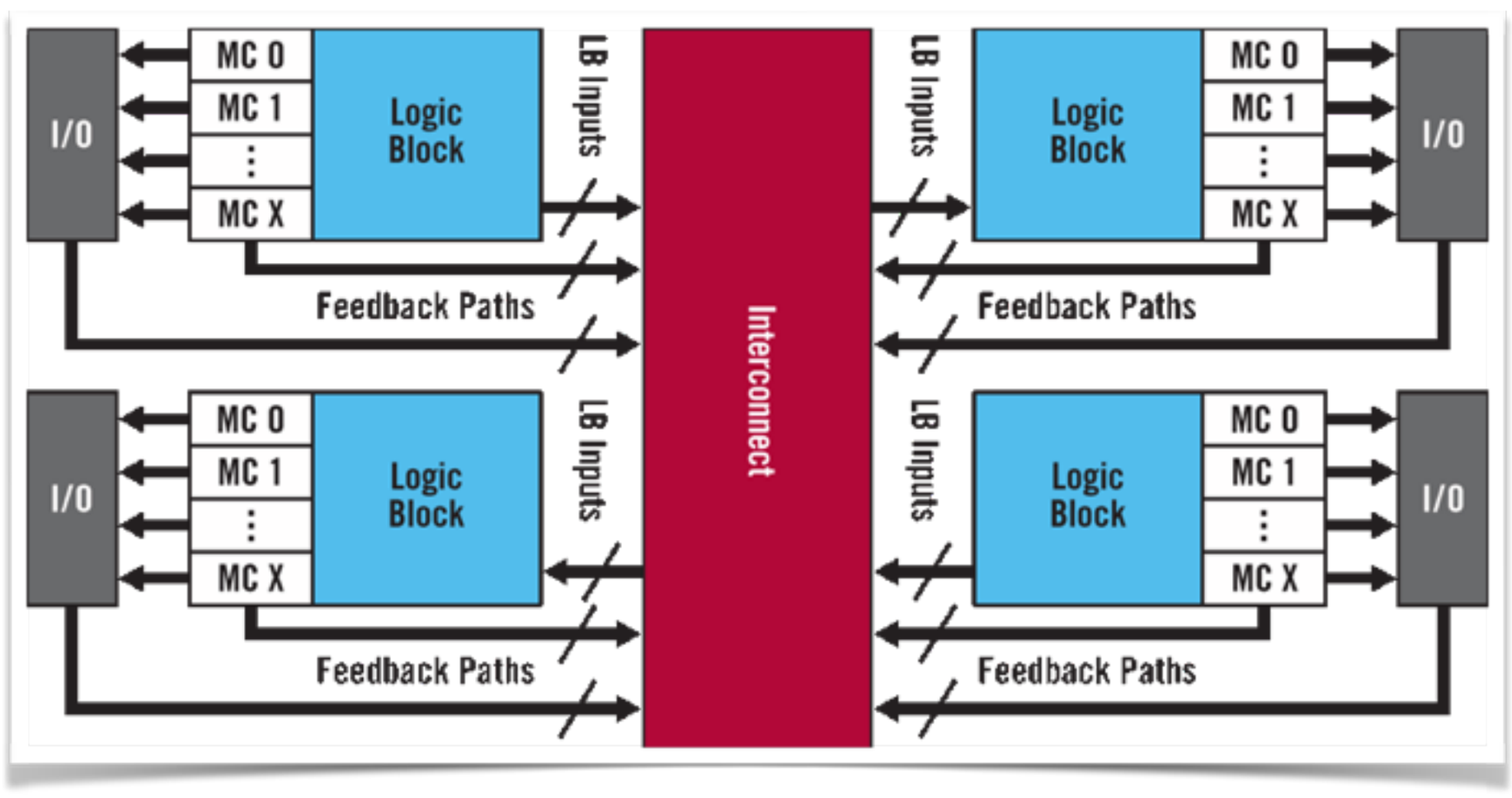
- **多**：功能强大 - 并大量并行处理结构
- **快**：开发快，上市时间短，适合原型设计或小批量产品
- **好**：重复编程/配置，灵活、快速
- **省**：省电、节省板卡空间，便于调试， 系统成本低

PLD结构

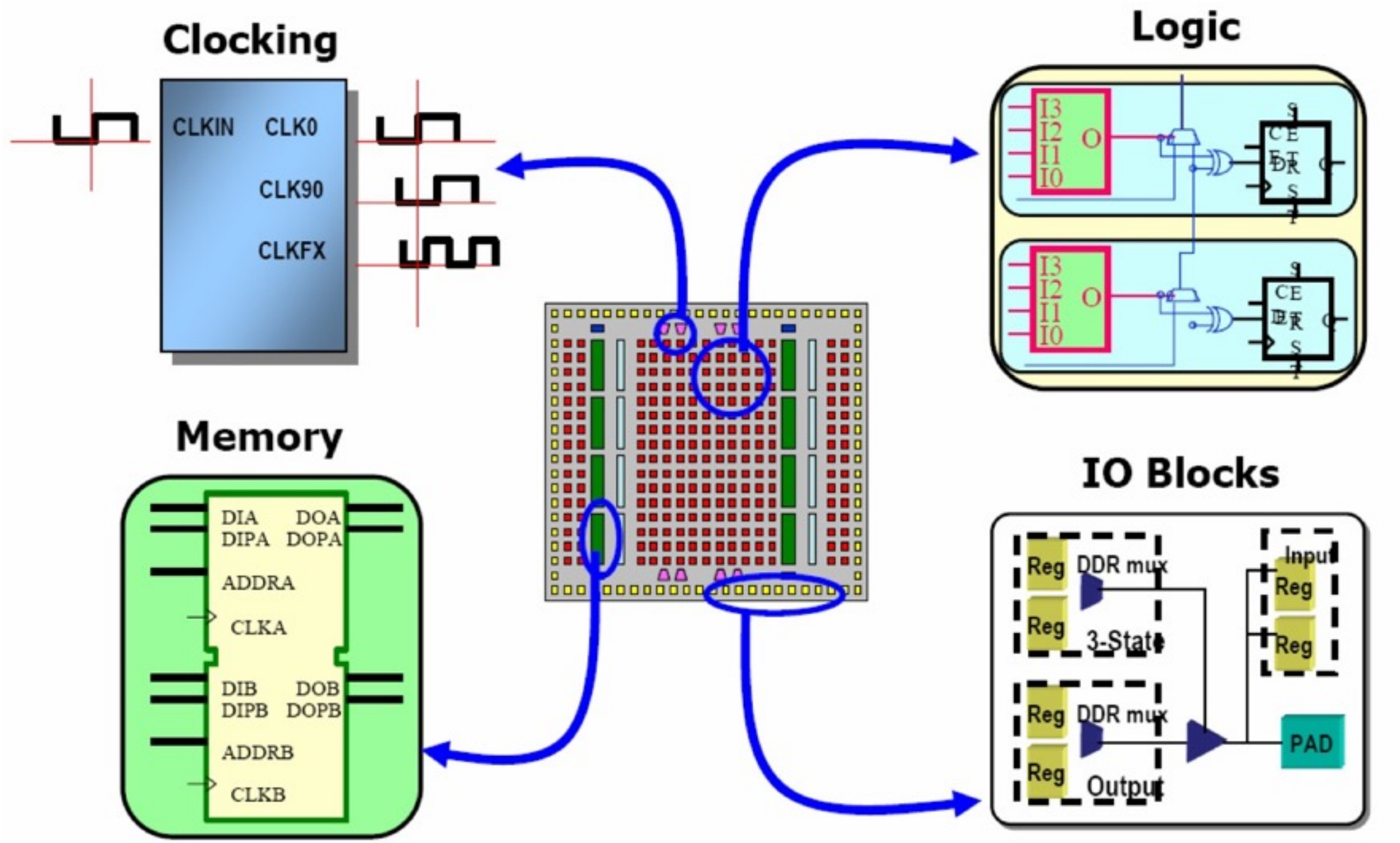


SPLD：单一与门/寄存器/反馈

CPLD：多个SPLD构成

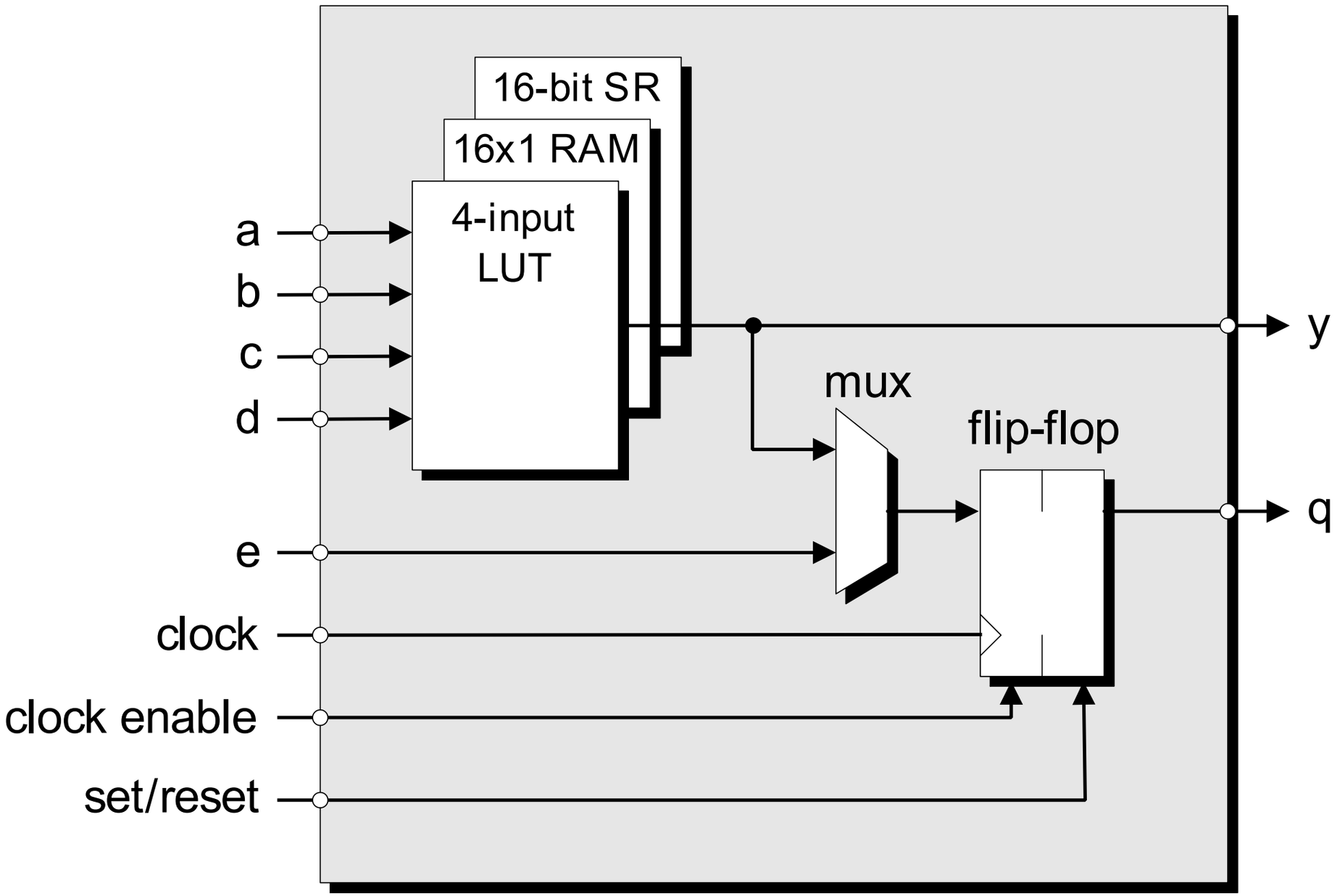


FPGA结构


Clocking
CLKIN
CLK0
CLK90
CLKFX
Logic
I3
I2
I1
I0
O
CE
D
R
S
Memory
DIA
DOA
DIPA
DOPA
ADDRA
CLKA
DIB
DOB
DIPB
DOPB
ADDRB
CLKB
IO Blocks
Reg
DDR mux
3-State
Input
Output
PAD

FPGA逻辑单元

- Xilinx：CLB/SLICE
- Altera：LE
- Lattice: LUTs/LCs



增强功能

- **内置处理器**：软核 & 硬核 & DSP
- **时钟及管理**：PLL、DLL、驱动 / 分配
- **IO**：多种高速收发、DDR存储器访问、可编程数控阻抗
- **嵌入MAC单元** – 高效浮点运算
- **各种内置存储器**：双口RAM、FIFO
- **各种常用接口**：I2C、SPI等
- **系统监控**：内置ADCs

主要供应商 － Altera

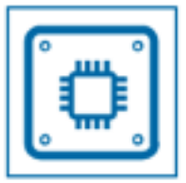
Altera headquarters in San Jose, California.

Type	Public
Traded as	NASDAQ: ALTR NASDAQ-100 Component S&P 500 Component
Industry	Integrated Circuits
Founded	1983
Headquarters	San Jose, California, U.S.
Key people	John P. Daane (Chairman, President and CEO)
Products	FPGAs, CPLDs, Embedded Processors, ASICs
Revenue	US$ 1.783 billion (2013)
Operating income	US$584.1 million (2013)
Net income	US$556.8 million (2013)
Total assets	US$4.658 billion (2013)
Total equity	US$3.333 billion (2013)
Number of employees	2,884 (December 2011)
Website	www.altera.com

- 主要产品：
  - FPGA： Stratix（高性能）、Arria（中端）、Cyclone（低成本）
  - PLD：MAX II、MAX V、MAX10
  - 电源：Enpirion PowerSoc DC－DC变换
- IP Core：
  - 软核：NIOS II、ColdFire V1、ARM Cortex M
  - 硬核：ARM Cortex A9
- 设计工具：
  - Quartus II

FPGAs

Stratix 10
Stratix V
Arria 10
Arria V
Cyclone V
MAX 10
All FPGAs »



SoCs

Stratix 10
Arria 10
Arria V
Cyclone V

SiP

Stratix 10 MX

CPLDs

MAX 10
MAX V
All CPLDs »

Configuration

Program Storage

Power

PowerSoC Converters
DDR Memory Termination
All Devices »

Intellectual Property

What's New in IP
Best in Class IP
Nios II Processor
Find IP
Reference Designs

Boards & Kits

Development Kits
Daughter Cards
Cables & Adapters
SoC System-on-Modules

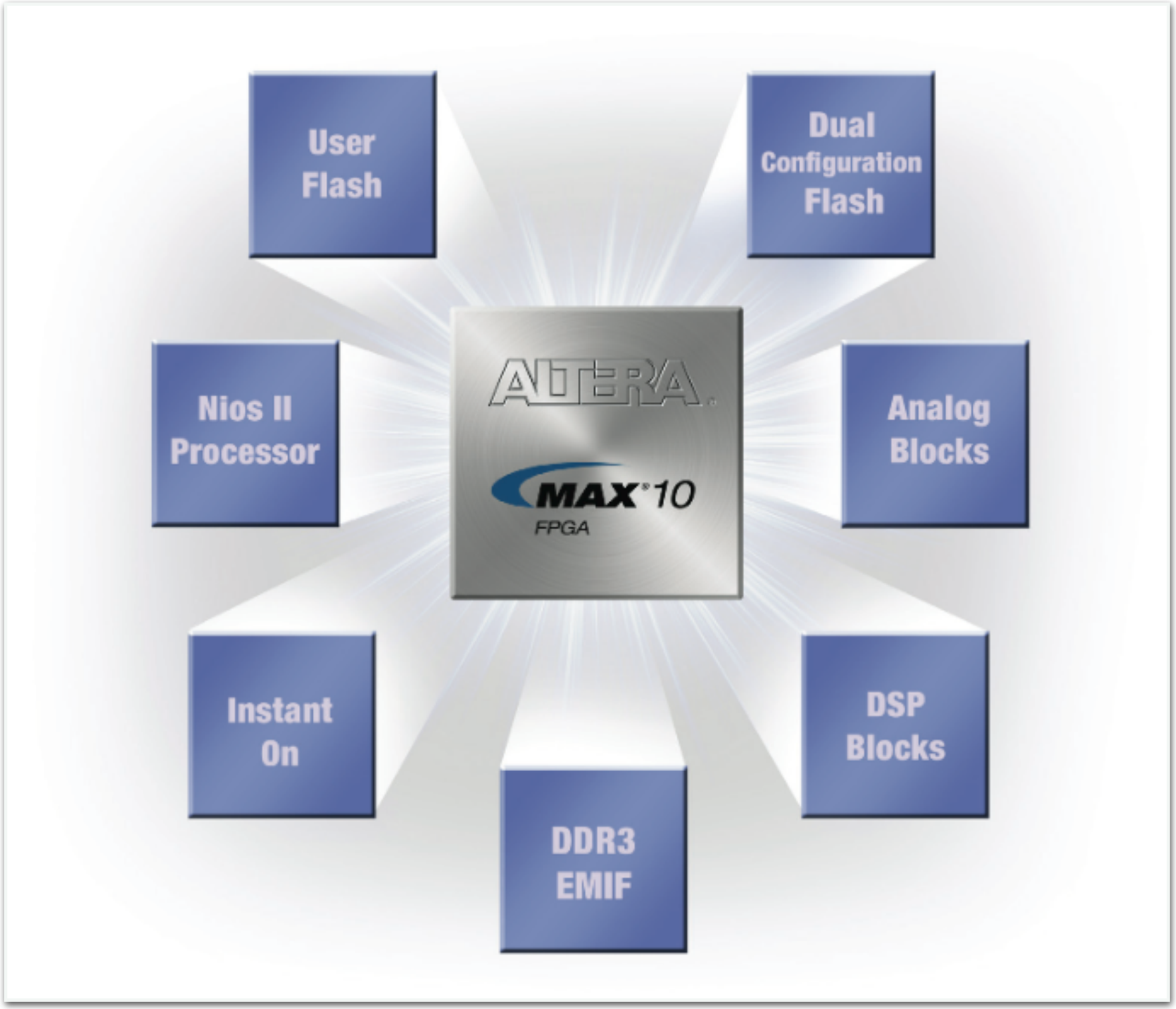
Design Software

What's New
Quartus Prime Software
Altera SDK for OpenCL
DSP Builder

SoC Development Tools

SoC EDS
ARM DS-5 AE

Altera典型产品 – MAX10



主要供应商 – Xilinx

XILINX

Xilinx headquarters in the United States.

Type	Public
Traded as	NASDAQ: XLNX NASDAQ-100 Component S&P 500 Component
Industry	Integrated Circuits
Founded	1984
Founder	Jim Barnett Ross Freeman Bernie Vonderschmitt
Headquarters	San Jose, California, U.S.
Area served	Worldwide
Key people	Philip T. Gianos Chairman of the Board Moshe N. Gavrielov President CEO Director
Products	FPGAs, CPLDs
Revenue	▲ US$ 2.382 billion (2014) [1] ▼ US$ 2.168 billion (2013) [1]
Operating income	▲ US$ 748.927 million (2014) [1] ▼ US$ 580.732 million (2013) [1]
Net income	▲ US$ 630.388 million (2014) [1] ▼ US$ 487.536 million (2013) [1]
Total assets	▲ US$ 5.037 billion (2014) [1] ▲ US$ 4.729 billion (2013) [1]

- FPGA发明者
- 第一个Fabless模式的半导体公司
- 主要产品：
  - FPGA： Virtex（高性能）、Kintex（中端）、Artix（低成本）
  - ZYNQ（SoC）
  - PLD：CoolRunner、9500
- 设计工具：
  - Xilinx ISE
  - Vivado Design Suite

应用领域

Enabling Smarter, Connected, and Differentiated Systems and Networks

5G

- Cloud RAN
- Massive MIMO
- Backhaul
- Fronthaul
- Baseband
- Small Cell

SDN/NFV

- IP Over OTN
- Intrusion Detection
- Load Balancing
- OpenFlow Acceleration
- Traffic Management
- QoS Provisioning

Video/Vision

- Machine Vision
- 8K Display & Transport
- Surveillance
- Military Vision Systems
- Drones

ADAS

- Surround View
- Collision Avoidance
- Semi Autonomous
- Self Parking
- Vehicle to Vehicle
- Augmented Display

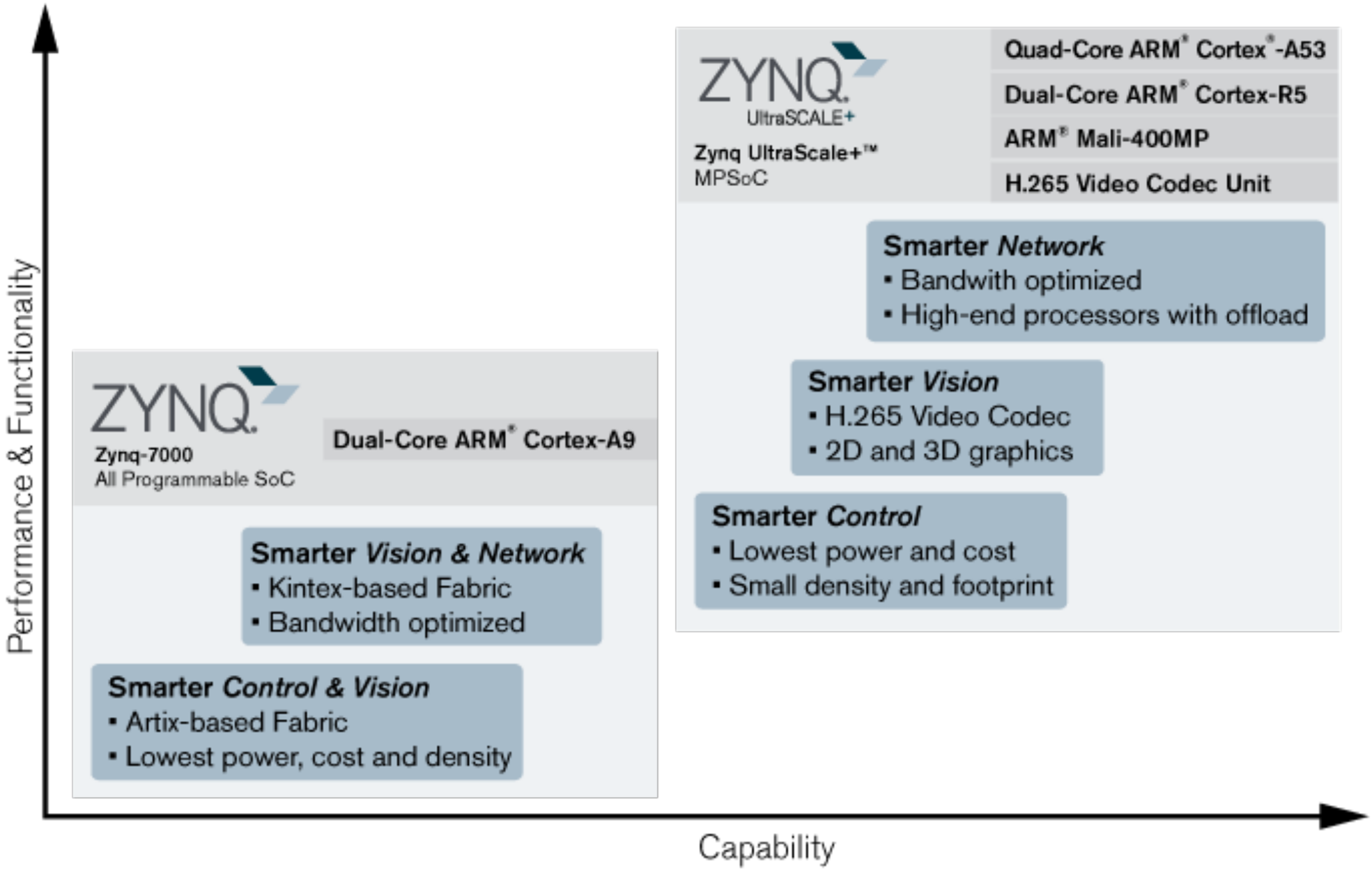
Industrial IoT

- Motion Control
- Machine-Machine
- Preventive Maintenance
- Smart Energy/Grid
- Smart Medical
- Big Data Analytics

Cloud Computing

- Cloud RAN
- Video in the Cloud
- Deep Neural Networks
- SSD Storage
- HFT - Financials
- Low Latency Caching

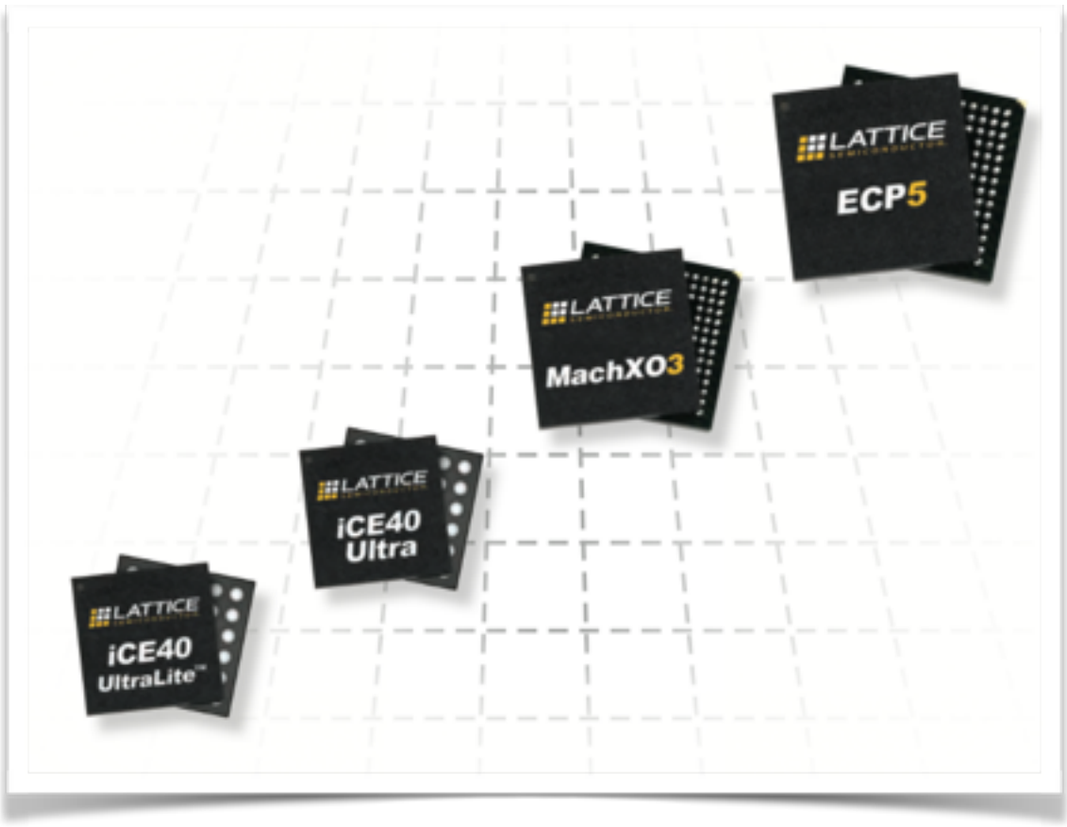
Xilinx典型产品 – ZYNQ



主要供应商 – Lattice Semi

LATTICE SEMICONDUCTOR

Type	Public (NASDAQ: LSCC)
Industry	Integrated Circuits
Founded	1983, public since 1989
Headquarters	Portland, Oregon, United States 45.527216°N 122.926626°W
Key people	Darin Billerbeck, CEO
Products	FPGAs, CPLDs
Revenue	$366.1 million (2014)[1]
Net income	▲ $48.6 million (2014)[1]
Number of employees	~1200 (2015)[1]
Website	www.latticesemi.com



- FPGA行业第三、PLD行业第二
- 主要产品：
  - iCE（世界最小）、MachXO（桥接、扩展）、ECP（连接、加速）
  - 电源管理：Power Manager、Platform Manager
  - 时钟管理：ispClock
- 设计工具：Lattice Diamond

主要供应商 – Actel(MicroSemi)

Actel®

Industry	Integrated Circuits
Founded	1985
Headquarters	Mountain View, CA, USA
Key people	John East, CEO & President Maurice Carson, CFO Esmat Hamdy, Sr. Vice President, Technology & Operations Jay Legenhausen, Sr. Vice President, Worldwide Sales Fares Mubarak, Sr. Vice President, Marketing & Engineering
Products	FPGAs, Embedded Processors
Operating income	▼ US$-21.3 Million *(FY 2009)*[1]
Net income	▼ US$-46.2 Million *(FY 2009)*[1]
Total assets	▼ US$307 Million *(FY 2009)*[2]
Total equity	▼ US$233 Million *(FY 2009)*[2]
Number of employees	500+[3]
Parent	Microsemi revenue = ▲ US$191 Million *(FY 2009)*[1]
Website	www.actel.com www.microsemi.com

FPGAs

IGLOO2 FPGAs

- Best-in-Class Integration, Low Power, Reliability and Security
- The IGLOO2 family offers unrivaled mainstream FPGA features including:
  - highest number of GPIOs for any given density node for 5G SERDES FPGAs;
  - highest number of 5G transceivers density
  - highest number of PCI compliant 3.3V I/Os in the industry
  - highest number of PCIe endpoints

» IGLOO2 FPGAs

Microsemi SoC/FPGAs for Secure Connectivity in IoT Applications

Learn More >>

IGLOO FPGAs

- Low Power FPGAs
- With Flash*Freeze technology
- Available with ARM® Cortex™-M1-enabled processor core

» IGLOO Overview » IGLOO/e» IGLOO nano » IGLOO PLUS

ProASIC3 FPGAs

- Low power FPGAs
- Available with Flash*Freeze technology
- Offered with ARM-enabled processor cores

» ProASIC3 Overview » ProASIC3/e » ProASIC3 nano » ProASIC3L

Fusion Mixed Signal FPGAs

- Mixed signal FPGAs with support for soft microcontroller cores such as ARM Cortex-M1, 8051, and CoreABC
- Programmable analog with ADC and voltage/current/temperature monitors
- Proven ProASIC3 FPGA fabric with up to 1.5M gates and 292 analog and digital I/Os

» Fusion

选型原则

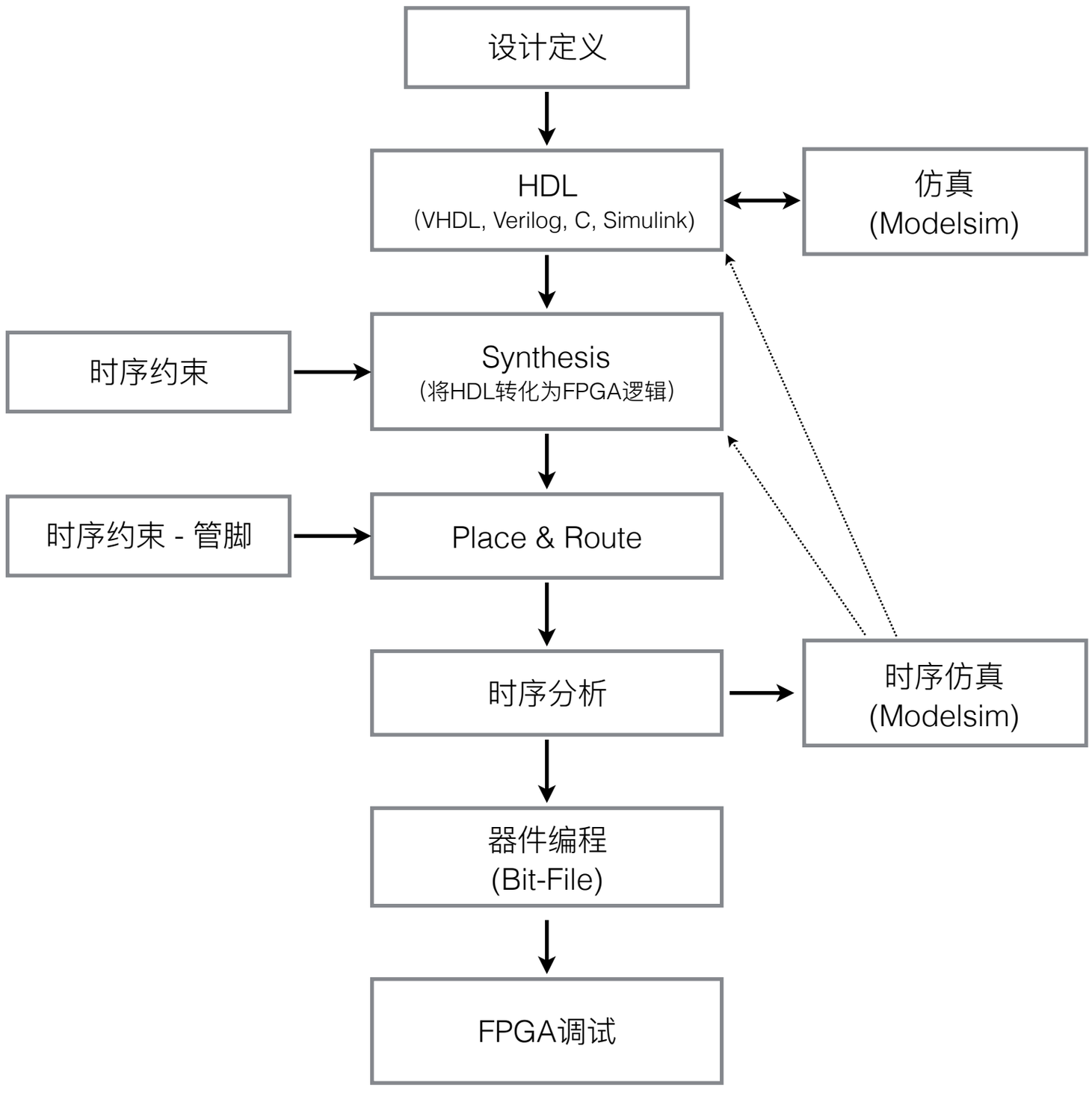
- **功能 / 资源**：逻辑单元、存储器、处理能力、IO、处理器内核、DSP
- **封装**：满足管脚数量以及板卡的物理尺寸要求
- **功耗**：满足系统对供电的限制需求
- **开发工具 / 难度**：影响设计难度和开发时间
- **系统成本**：包括配置RAM、外供电源、时钟等
- **购买难度**：价钱 / 数量 / 供货渠道

Lattice MachXO2 FPGA

MachXO2 Device Selection Guide

	XO2-256	XO2-640	XO2-640U	XO2-1200	XO2-1200U	XO2-2000	XO2-2000U	XO2-4000	XO2-7000
Density LUTs	256	640	640	1280	1280	2112	2112	4320	6864
EBR RAM Blocks (9 Kbits/block)	0	2	7	7	8	8	10	10	26
EBR SRAM (Kbits)	0	18	64	64	74	74	92	92	240
Dist. SRAM (Kbits)	2	5	5	10	10	16	16	34	54
User Flash Memory (Kbits)	0	24	64	64	80	80	96	96	256
PLL + DLL	0	0	1 + 2	1 + 2	1 + 2	1 + 2	2 + 2	2 + 2	2 + 2
DDR/DDR2/LPDDR Memory Support	-	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Configuration Memory	Internal Flash								
Dual Boot[1]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Embedded Function Blocks	I2C (2), SPI (1), Timer (1)								
Core Vcc 1.2 V	ZE	ZE	-	ZE	-	ZE & HE	HE	ZE & HE	ZE & HE
Core Vcc 2.5 - 3.3 V	HC	HC	HC	HC	HC	HC	HC	HC	HC
Temp C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temp I	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

设计流程


设计定义
HDL
(VHDL, Verilog, C, Simulink)
仿真
(Modelsim)
时序约束
Synthesis
(将HDL转化为FPGA逻辑)
时序约束 - 管脚
Place & Route
时序分析
时序仿真
(Modelsim)
器件编程
(Bit-File)
FPGA调试

硬件设计注意

- **管脚分配**：输入/输出类型，预留功能管脚，方便布线
- **时钟**：全局时钟 vs 局部时钟，PLL vs DLL，是否驱动
- **电源**：内核电压 / 接口电压及其相应电流，上电时序
- **编程**：JTAG、配置、在线更新
- **测试点**：关键信号 – 时钟、电源、关键IO

逻辑设计注意

» 善用**IP Core**：调用原厂提供的经过验证过的IP内核

» **硬件设计概念**：并行工作、时延

» **充分仿真**：功能仿真、时序仿真、TestBench

» **调试**：使用原厂提供的片上逻辑分析工具

V•T•E	Programmable logic		[hide]
Concepts	ASIC · SOC · FPGA (Logic block) · CPLD · EPLD · PLA · PAL · GAL · Reconfigurable computing (Xputer) · Soft microprocessor · Circuit underutilization		
Languages	Verilog (A · AMS · Icarus) · VHDL (AMS · VITAL) · SystemVerilog (DPI) · SystemC · AHDL · Handel-C · PSL · UPF · PALASM · ABEL · CUPL · PSHDL · OpenVera · C to HDL · Flow to HDL · MyHDL · JHDL · ELLA		
Companies	Accellera · **Actel** · Achronix · AMD · Aldec · Altera · Atmel · Cadence · Cypress · Duolog · Forte · Intel · Lattice · National · Mentor Graphics · Microsemi · Signetics · Synopsys (Magma · Virage Logic) · Texas Instruments · Tabula · Xilinx		
Products	**Hardware**	Stratix · Virtex (FPGA)	
	Software	Altera Quartus · Xilinx ISE · ModelSim · Simulators	
	IP	**Proprietary**	ARC · LEON · LatticeMico32 · MicroBlaze · PicoBlaze · Nios · Nios II
		Open-source	LatticeMico8 · OpenCores · OpenRISC (1200) · RISC-V · JOP

充分利用设计资源

工具

- 开发板/评估板
- 调试工具
- 编译/仿真软件

IP Cores

- 原厂官方提供
- 开源组织提供
- 其它人验证

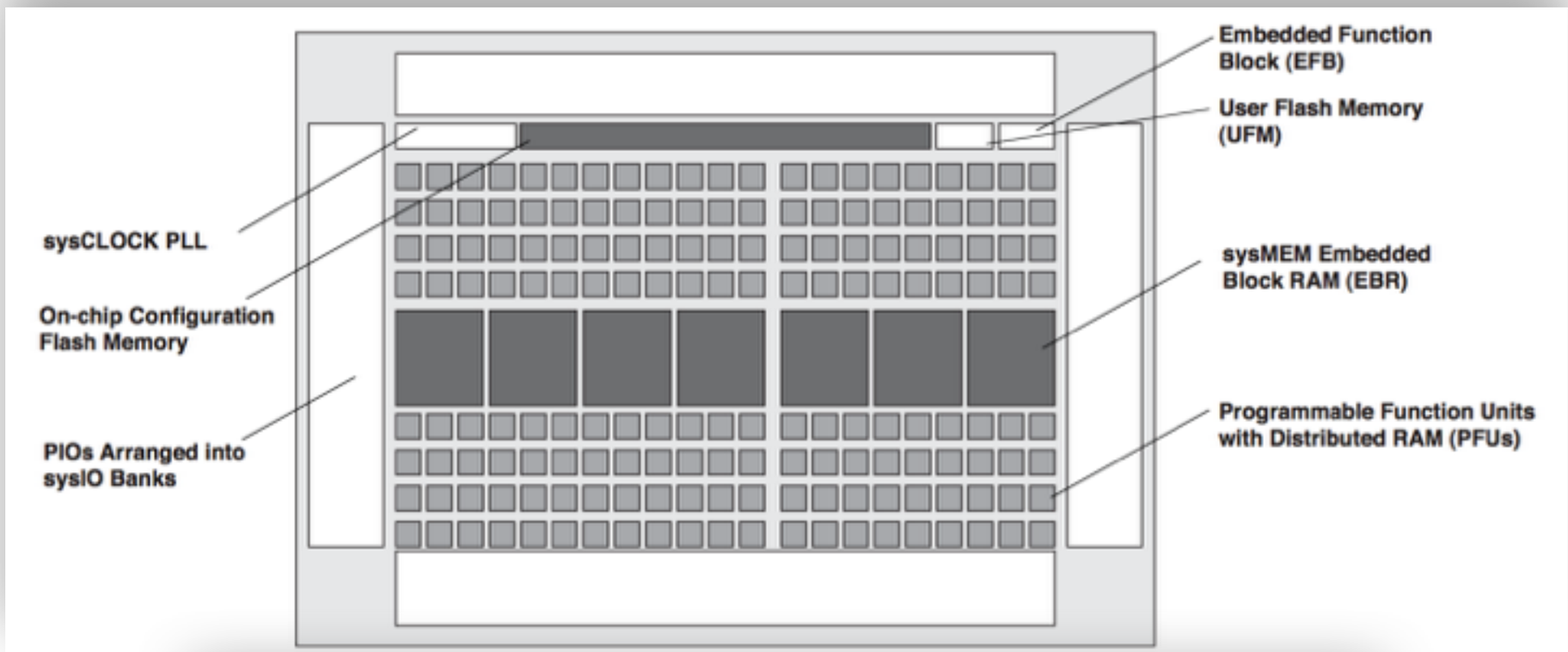
参考

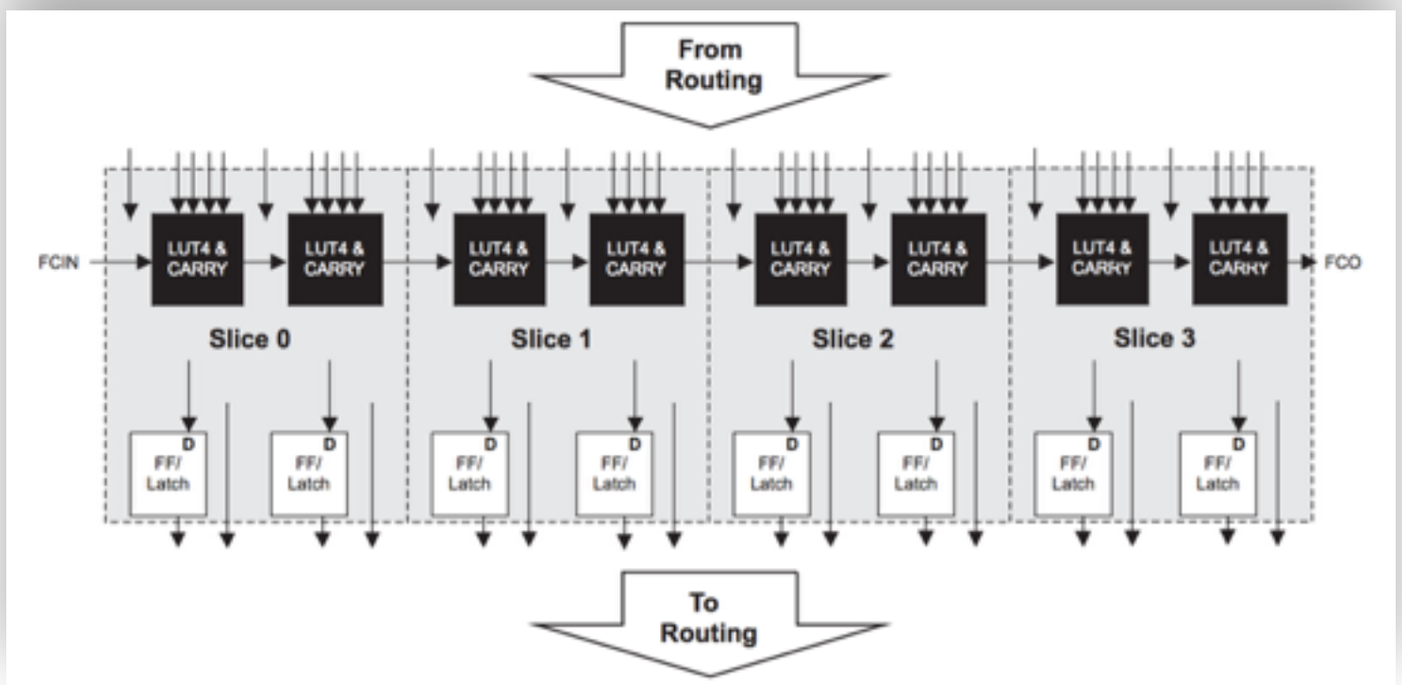
- 设计指南
- 系统应用
- 视频/教程

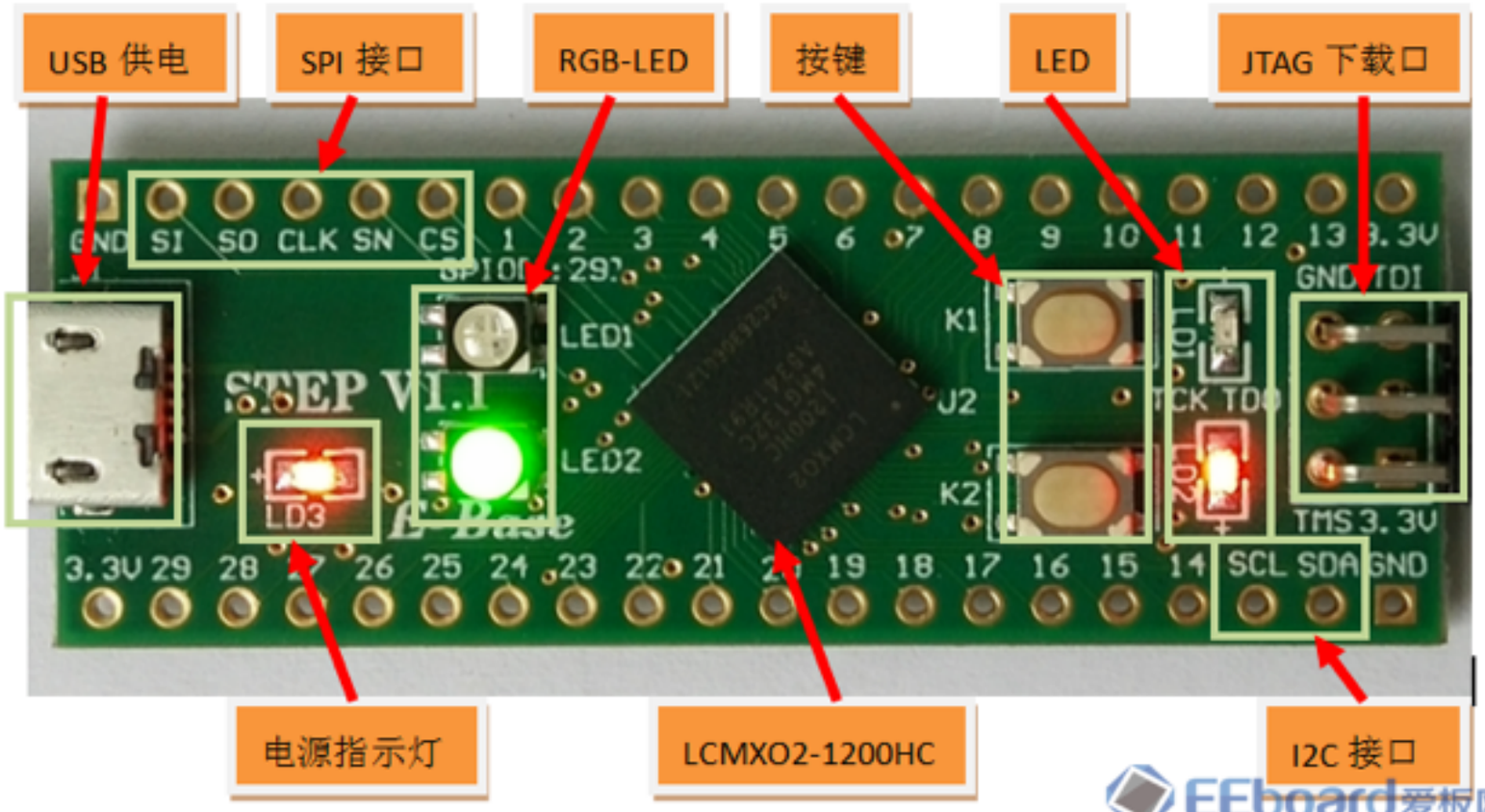
技术支持

- 原厂FAE
- 第三方机构
- 论坛/社区

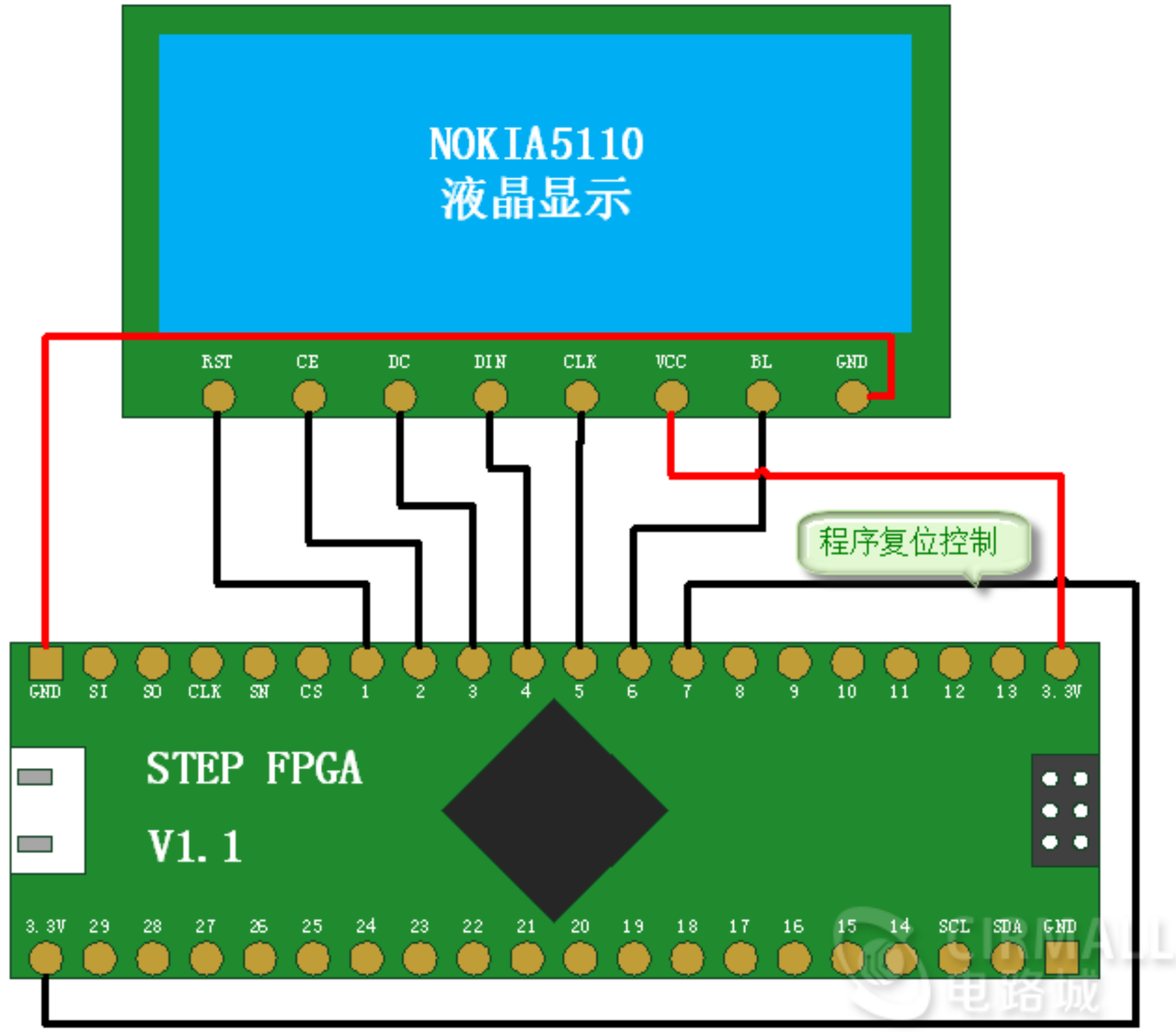
MACHXO2


Embedded Function Block (EFB)
User Flash Memory (UFM)
sysCLOCK PLL
On-chip Configuration Flash Memory
sysMEM Embedded Block RAM (EBR)
PIOs Arranged into sysIO Banks
Programmable Function Units with Distributed RAM (PFUs)

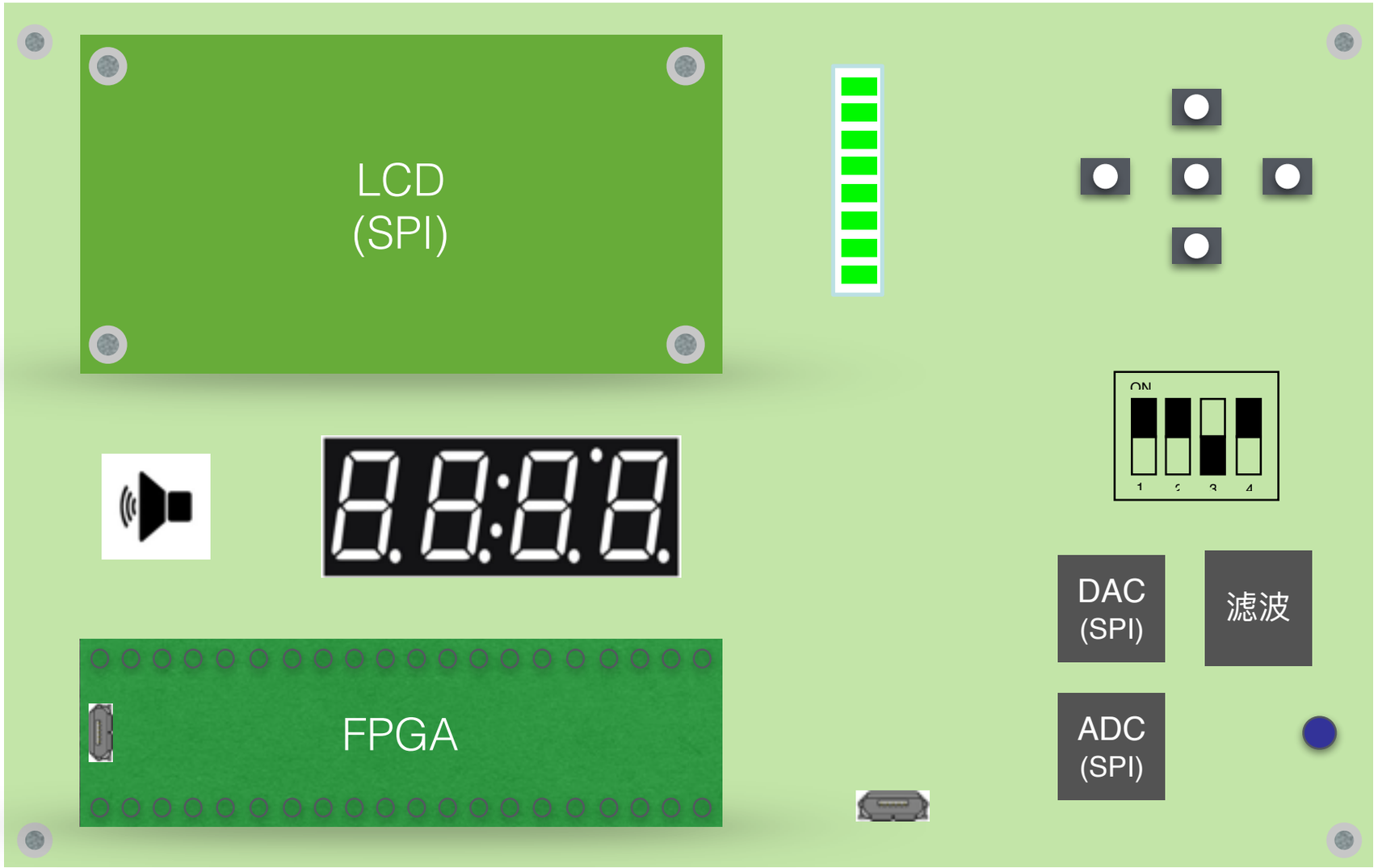

From Routing
FCIN
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
LUT4 & CARRY
FCO
Slice 0
Slice 1
Slice 2
Slice 3
D
FF/ Latch
To Routing



- FPGA芯片：LCMXO2-1200HC-4MG132
- 通过USB 5V供电
- 板上有25MHz时钟
- 3个LED，一路电源指示，两路用户LED
- 2个按键
- 2个RGB LED
- 一路I2C接口
- SPI接口（可设主从模式）
- JTAG接口
- 29个GPIO接口

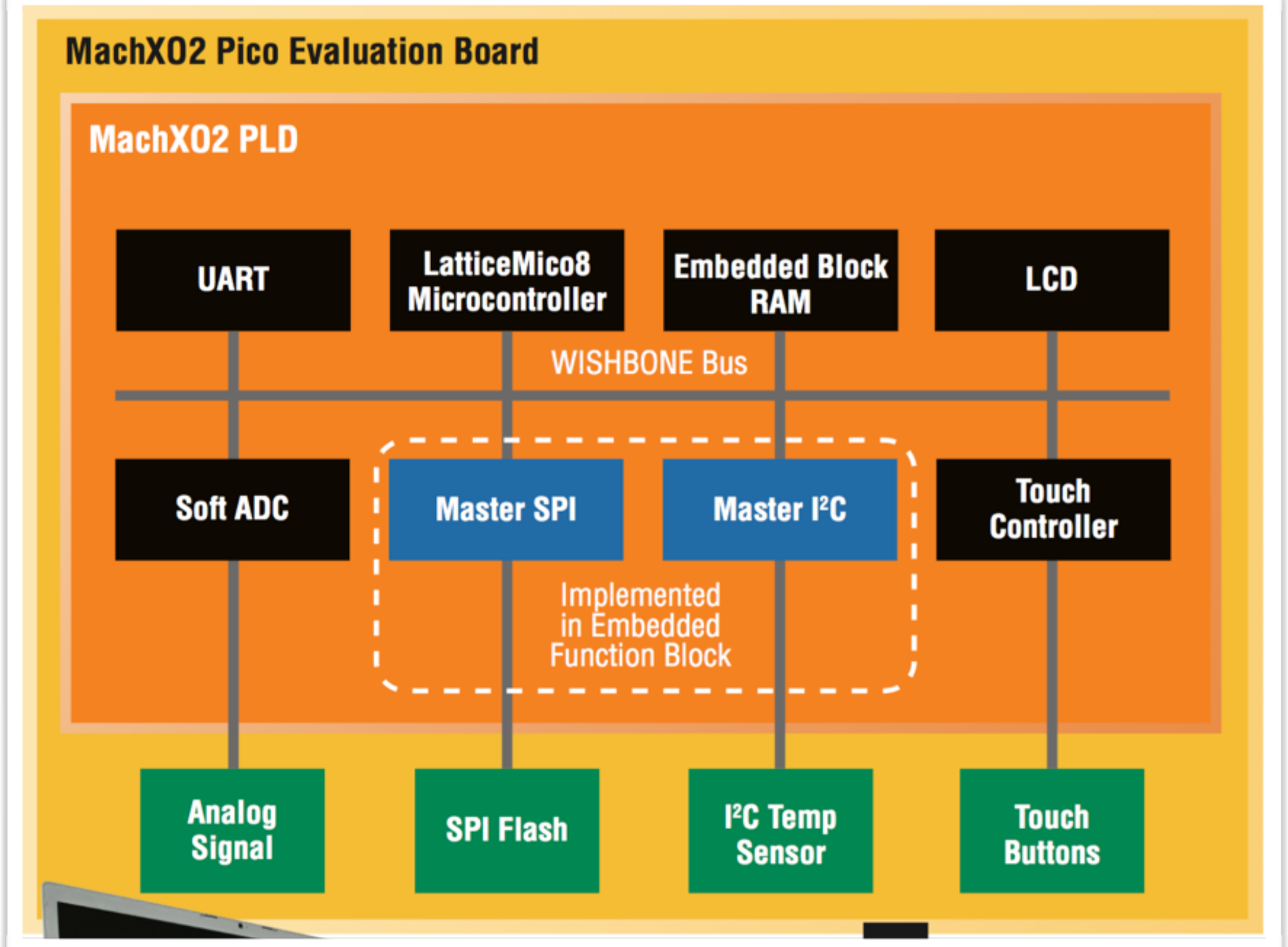

NOKIA5110
液晶显示
RST
CE
DC
DIN
CLK
VCC
BL
GND
程序复位控制
GND
SI
SO
CLK
SN
CS
1
2
3
4
5
6
7
8
9
10
11
12
13
3.3V
STEP FPGA
V1.1
3.3V
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
SCL
SDA
GND

系统训练平台



技能训练

- **FPGA使用**
- **Verilog设计**
- **输入：按键 / 开关**
- **输出：LED、数码管、LCD**
- **DDS / 信号产生**
- **数据采集 / ADC**
- **串行总线SPI / I2C**
- **数据类型处理**
- **FPGA IP内核使用**
- **存储器设计 – ROM / FIFO**
- **8位单片机软核使用**


MachXO2 Pico Evaluation Board
MachXO2 PLD
UART
LatticeMico8 Microcontroller
Embedded Block RAM
LCD
WISHBONE Bus
Soft ADC
Master SPI
Master I²C
Touch Controller
Implemented in Embedded Function Block
Analog Signal
SPI Flash
I²C Temp Sensor
Touch Buttons