# SECTION 6
HIGH SPEED DACs AND DDS SYSTEMS
Walt Kester

INTRODUCTION

A frequency synthesizer generates multiple frequencies from one or more frequency references. These devices have been used for decades, especially in communications systems. Many are based upon switching and mixing frequency outputs from a bank of crystal oscillators. Others have been based upon well understood techniques utilizing phase-locked loops (PLLs). This mature technology is illustrated in Figure 6.1. A fixed-frequency reference drives one input of the phase comparator. The other phase comparator input is driven from a divide-by-N counter which is in turn driven by a voltage-controlled-oscillator (VCO). Negative feedback forces the output of the internal loop filter to a value which makes the VCO output frequency N-times the reference frequency. The time constant of the loop is controlled by the loop filter. There are many tradeoffs in designing a PLL, such a phase noise, tuning speed, frequency resolution, etc., and there are many good references on the subject (see References 1, 2, and 3).

## FREQUENCY SYNTHESIS USING
OSCILLATORS AND PHASE-LOCKED LOOPS
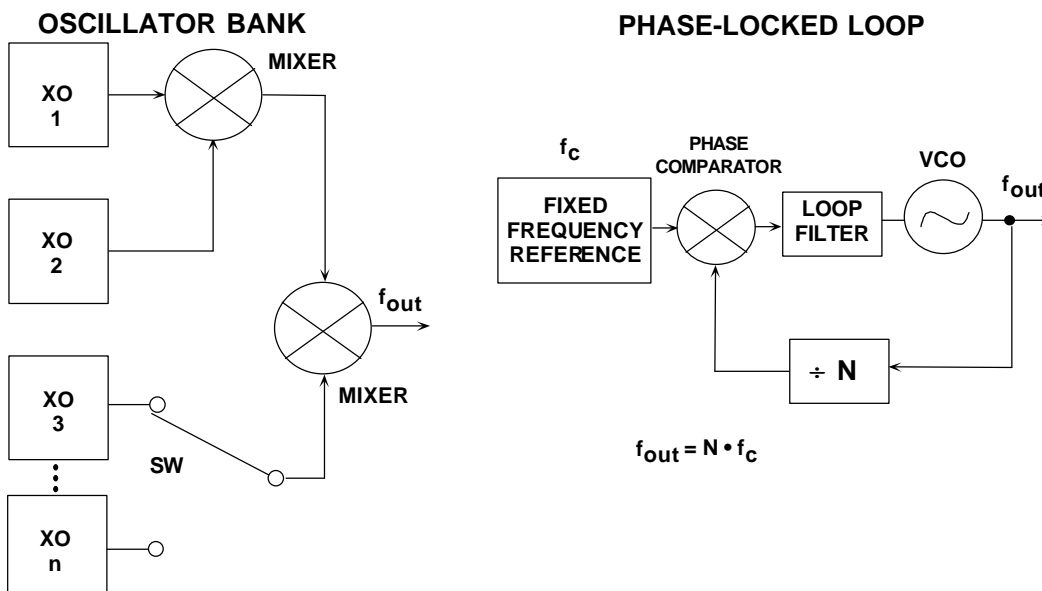
6.1

With the widespread use of digital techniques in instrumentation and communications systems, a digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The basic architecture is shown in Figure 6.2. In this simplified model, a stable clock drives a programmable-read-only-memory (PROM) which stores one or more integral number of cycles of a sinewave (or other arbitrary

waveform, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal. The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock.

The DDS system differs from the PLL in several ways. Because a DDS system is a sampled data system, all the issues involved in sampling must be considered: quantization noise, aliasing, filtering, etc. For instance, the higher order harmonics of the DAC output frequencies fold back into the Nyquist bandwidth, making them unfilterable, whereas, the higher order harmonics of the output of PLL-based synthesizers can be filtered. There are other considerations which will be discussed shortly.
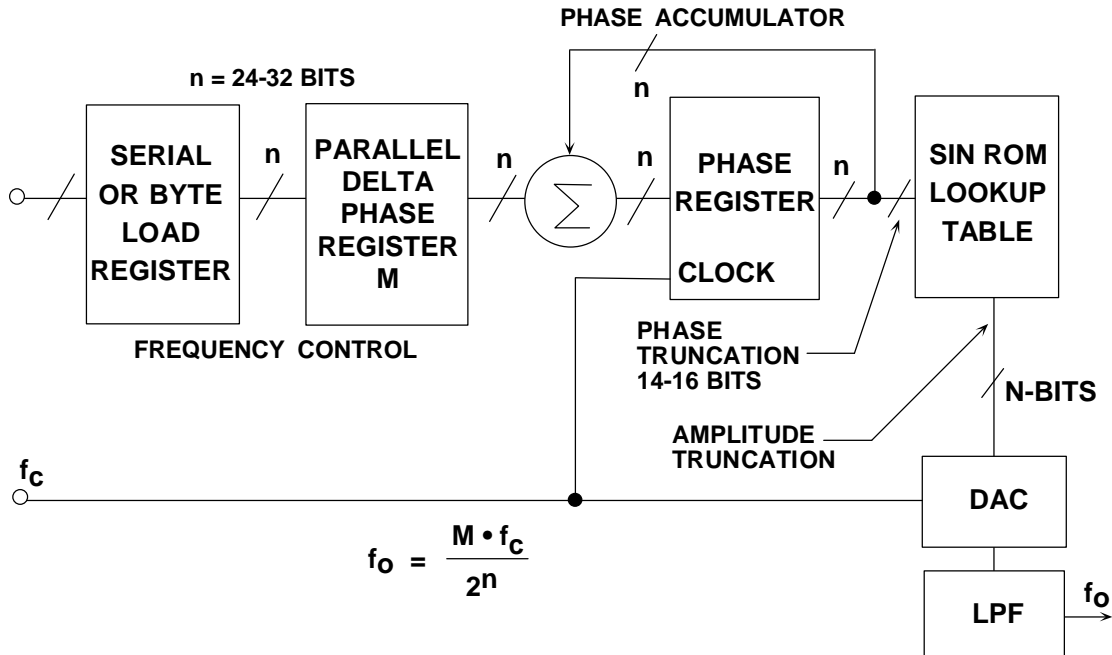
FUNDAMENTAL DIRECT DIGITAL SYNTHESIS SYSTEM

■ LOOKUP TABLE CONTAINS SIN DATA FOR INTEGRAL NUMBER OF CYCLES
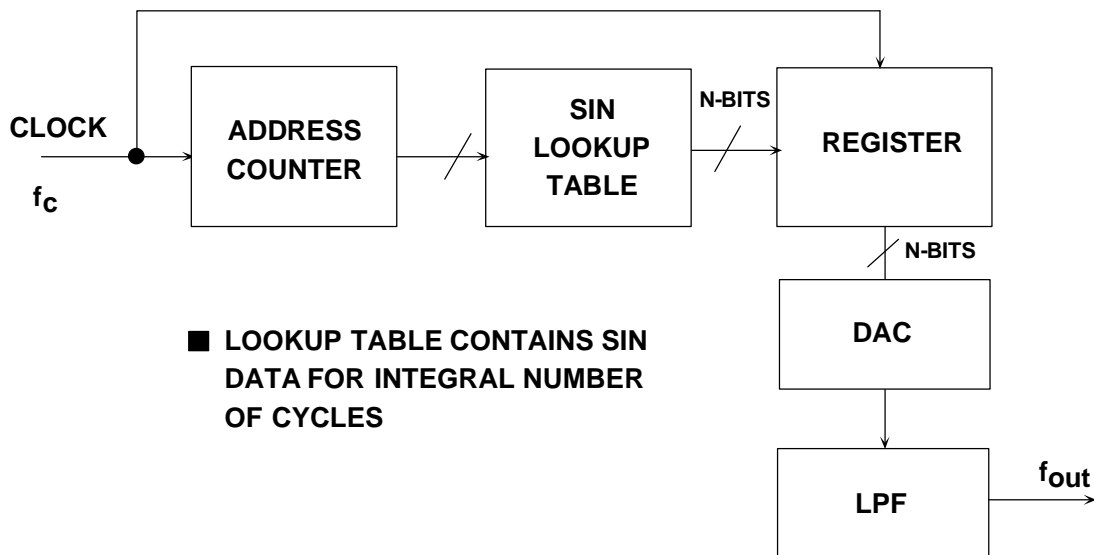
ANALOG DEVICES   **6.2**

A fundamental problem with this simple DDS system is that the final output frequency can be changed only by changing the reference clock frequency or by reprogramming the PROM, making it rather inflexible. A practical DDS system implements this basic function in a much more flexible and efficient manner using digital hardware called a Numerically Controlled Oscillator (NCO). A block diagram of such a system is shown in Figure 6.3.

A FLEXIBLE DDS SYSTEM

PHASE ACCUMULATOR

n = 24-32 BITS

SERIAL OR BYTE LOAD REGISTER	n	PARALLEL DELTA PHASE REGISTER M	n	Σ	n	PHASE REGISTER CLOCK	n	SIN ROM LOOKUP TABLE

n

FREQUENCY CONTROL

PHASE TRUNCATION 14-16 BITS

AMPLITUDE TRUNCATION

N-BITS

f_C

DAC

$$f_O = \frac{M \cdot f_C}{2^n}$$

LPF f_O

6.3

The heart of the system is the *phase accumulator* whose contents is updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the *delta phase register* is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator is 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, 2^{32} clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. (Actually, only data for 90° is required because the quadrature data is contained in the two MSBs). The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC.

Consider the case for n=32, and M=1. The phase accumulator steps through each of 2^{32} possible outputs before it overflows. The corresponding output sinewave frequency is equal to the clock frequency divided by 2^{32}. If M=2, then the phase accumulator register "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows.

For an n-bit phase accumulator (n generally ranges from 24 to 32 in most DDS systems), there are 2^n possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If f_C is the clock frequency, then the frequency of the output sinewave is equal to:

$$f_0 = \frac{M \cdot f_c}{2^n}.$$

This equation is known as the DDS "tuning equation." Note that the frequency resolution of the system is equal to $f_c/2^n$. For n=32, the resolution is greater than one part in four billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are truncated, leaving only the first 13 to 15 MSBs. This reduces the size of the lookup table and does not affect the frequency resolution. The phase truncation only adds a small but acceptable amount of phase noise to the final output.

The resolution of the DAC is typically 2 to 4 bits less than the width of the lookup table. Even a perfect N-bit DAC will add quantization noise to the output. Figure 6.4 shows the calculated output spectrum for a 32-bit phase accumulator, 15-bit phase truncation, and a 12-bit DAC. The value of M was chosen so that the output frequency was slightly offset from 0.25 times the clock frequency. Note that the spurs caused by the phase truncation and the finite DAC resolution are all at least 90dB below the fullscale output. This performance far exceeds that of any commercially available 12-bit DAC and is adequate for most applications.

CALCULATED OUTPUT SPECTRUM SHOWS
90dB SFDR FOR 15-BIT PHASE TRUNCATION AND
## 12-BIT OUTPUT DATA TRUNCATION

ANALOG
DEVICES
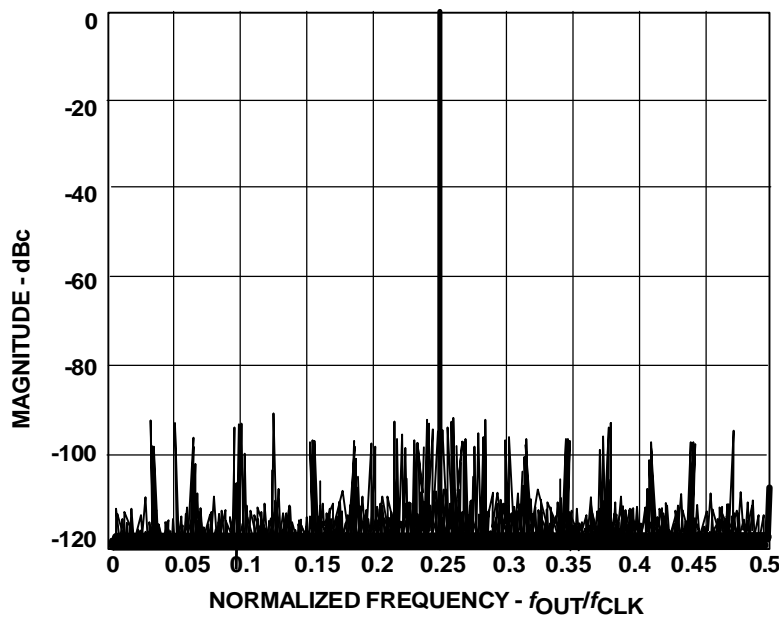
6.4

The basic DDS system described above is extremely flexible and has high resolution. The frequency can be changed instantaneously with no phase discontinuity by simply changing the contents of the M-register. However, practical DDS systems first require the execution of a serial, or byte-loading sequence to get the new frequency word into an internal buffer register which precedes the parallel-output M-register. This is done to minimize package pin count. After the new word is loaded

into the buffer register, the parallel-output delta phase register is clocked, thereby changing all the bits simultaneously. The number of clock cycles required to load the delta-phase buffer register determines the maximum rate at which the output frequency can be changed.

ALIASING IN DDS SYSTEMS

There is one important limitation to the range of output frequencies that can be generated from the simple DDS system. The Nyquist Criteria states that the clock frequency (sample rate) must be at least twice the output frequency. Practical limitations restrict the actual highest output frequency to about 1/3 the clock frequency. Figure 6.5 shows the output of a DAC in a DDS system where the output frequency is 30MHz and the clock frequency is 100MHz. An antialiasing filter must follow the reconstruction DAC to remove the lower image frequency (100– 30=70MHz) as shown in the figure.

ALIASING IN A DDS SYSTEM

ANALOG
DEVICES
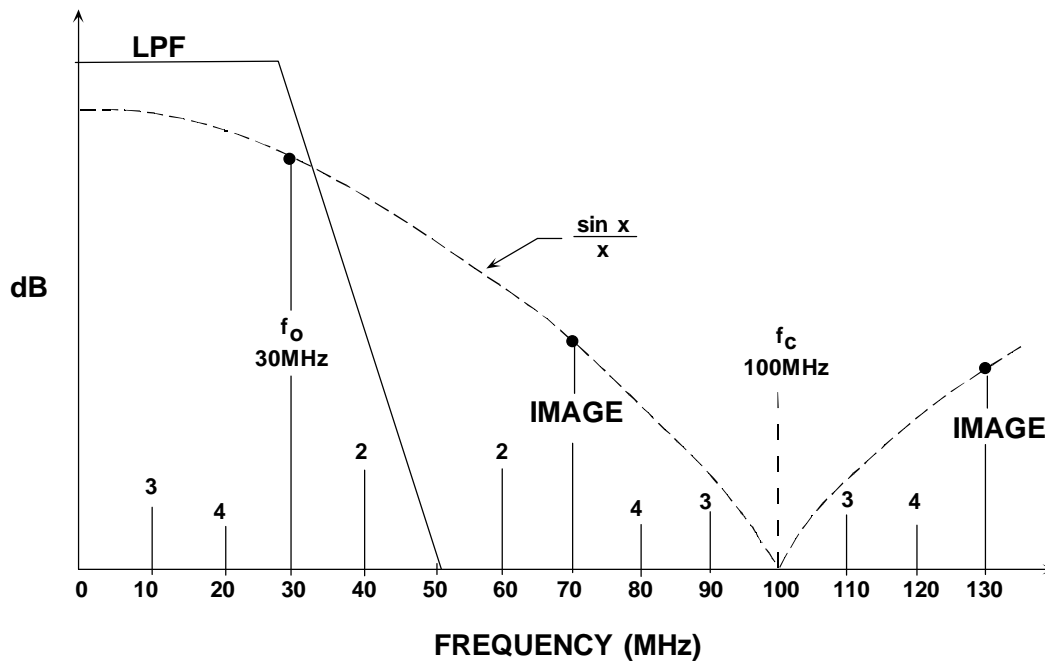
6.5

Note that the amplitude response of the DAC output (before filtering) follows a sin(x)/x response with zeros at the clock frequency and multiples thereof. The exact equation for the normalized output amplitude, $A(f_0)$, is given by:

$$A(f_0) = \frac{\sin\left(\dfrac{\pi f_0}{f_c}\right)}{\dfrac{\pi f_0}{f_c}},$$

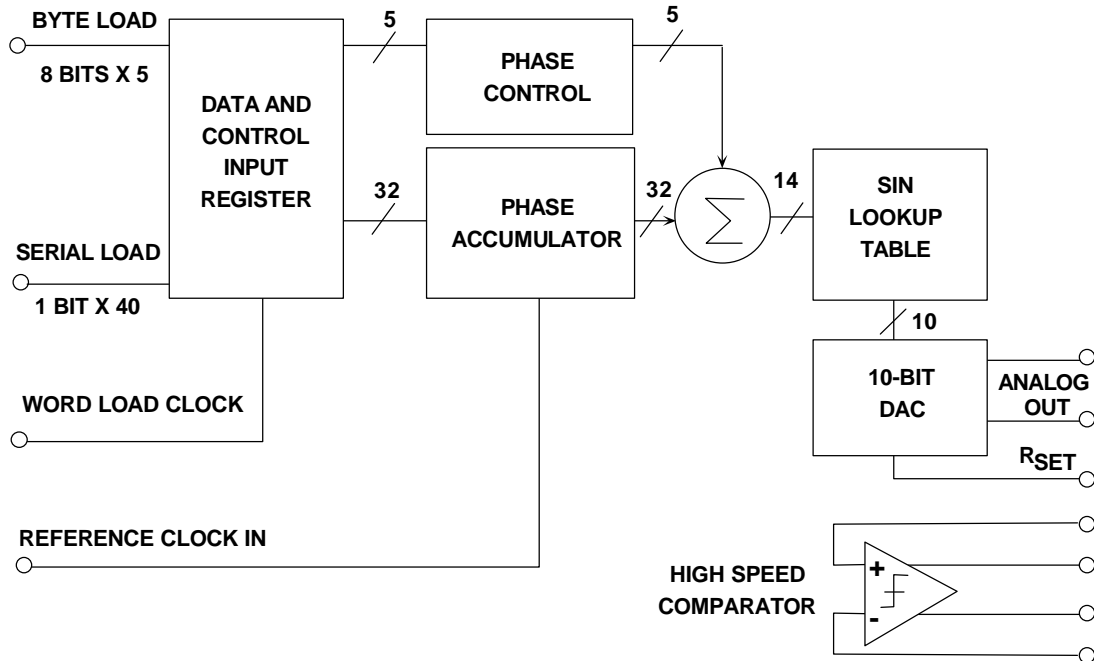where f_0 is the output frequency and f_c is the clock frequency.

5

This rolloff is because the DAC output is not a series of zero-width impulses (as in a perfect re-sampler), but a series of rectangular pulses whose width is equal to the reciprocal of the update rate. The amplitude of the sin(x)/x response is down 3.92dB at the Nyquist frequency (1/2 the DAC update rate). In practice, the transfer function of the antialiasing filter is designed to compensate for the sin(x)/x rolloff so that the overall frequency response is relatively flat up to the maximum output DAC frequency (generally 1/3 the update rate).

Another important consideration is that, unlike a PLL-based system, the higher order harmonics of the fundamental output frequency in a DDS system will fold back into the baseband because of aliasing. These harmonics cannot be removed by the antialiasing filter. For instance, if the clock frequency is 100MHz, and the output frequency is 30MHz, the second harmonic of the 30MHz output signal appears at 60MHz (out of band), but also at 100–60=40MHz (the aliased component. Similarly, the third harmonic (90MHz) appears inband at 100–90=10MHz, and the fourth at 120–100MHz=20MHz. Higher order harmonics also fall within the Nyquist bandwidth (DC to $f_c/2$). The location of the first four harmonics is shown in the diagram.

125MSPS DDS SYSTEM (AD9850)

The AD9850 125MSPS DDS system (Figure 6.6) uses a 32-bit phase accumulator which is truncated to 14-bits (MSBs) before being passed to the lookup table. The final digital output is 10-bits to the internal DAC. The AD9850 allows the output phase to be modulated using an additional register and an adder placed between the output of the phase accumulator register and the input to the lookup table. The AD9850 uses a 5-bit word to control the phase which allows shifting the phase in increments of 180°, 90°, 45°, 22.5°, 11.25°, and any combination thereof. The device also contains an internal high speed comparator which can be configured to accept the (externally) filtered output of the DAC to generate a low-jitter output pulse suitable for driving the sampling clock input of an ADC. The full scale output current can be adjusted from 10 to 20mA using a single external resistor, and the output voltage compliance is +1V. Key specifications are summarized in Figure 6.7.

AD9850 CMOS 125MSPS DDS/DAC SYNTHESIZER

BYTE LOAD

8 BITS X 5

DATA AND CONTROL INPUT REGISTER

5 → PHASE CONTROL 5

32 → PHASE ACCUMULATOR 32 → Σ → 14 → SIN LOOKUP TABLE

10 → 10-BIT DAC → ANALOG OUT

R_SET

SERIAL LOAD

1 BIT X 40

WORD LOAD CLOCK

REFERENCE CLOCK IN

HIGH SPEED COMPARATOR

6.6

AD9850 DDS/DAC SYNTHESIZER KEY SPECIFICATIONS

■ **125MSPS Clock Rate**

■ **On-Chip 10-bit DAC and High Speed Comparator**

■ **DAC SFDR > 50dBc @ 40MHz Output**

■ **32-bit Frequency Tuning**

■ **5-bit Phase Modulation**

■ **Simplified Control Interface: Byte-Parallel or Serial Load**

■ **+5V or +3.3V Supplies**

■ **380mW Dissipation @ 125MSPS on +5V Supply (30mW Power-Down Mode)**

■ **28-Pin Shrink Small Outline Package (SSOP)**

6.7

The frequency tuning (delta-phase register input word) and phase modulation words are loaded into the AD9850 via a parallel or serial loading format. The parallel load

format consists of five consecutive loads of an 8-bit control word (byte). The first 8-bit byte controls phase modulation (5-bits), power-down enable (1-bit), and loading format (2-bits). Bytes 2-5 comprise the 32-bit frequency tuning word. The maximum control register update frequency is 23MHz. Serial loading of the AD9850 is accomplished via a 40-bit serial data stream on a single pin. Maximum update rate of the control register in the serial-load mode is 3MHz.

The AD9850 consumes only 380mW of power on a single +5V supply at a maximum 125MSPS clock rate. The device is available in a 28-pin surface mount SSOP (Shrink Small Outline Package).

DDS SYSTEMS AS ADC CLOCK DRIVERS

DDS systems such as the AD9850 provide an excellent method of generating the sampling clock to the ADC, especially when the ADC sampling frequency must be under software control and locked to the system clock (see Figure 6.8). The *true* DAC output current I_{out}, drives a 200Ω, 42MHz lowpass filter which is source and load terminated, thereby making the equivalent load 100Ω. The filter removes spurious frequency components above 42MHz. The filtered output drives one input of the AD9850 internal comparator. The *complementary* DAC output current drives a 100Ω load. The output of the 100kΩ resistor divider placed between the two outputs is decoupled and generates the reference voltage for the internal comparator.

The comparator output has a 2ns rise and fall time and generates a TTL/CMOS-compatible square wave. The jitter of the comparator output edges is less than 20ps rms. True and complementary outputs are available if required.

In the circuit shown (Figure 6.8), the total output rms jitter for a 40MSPS ADC clock is 50ps rms, and the resulting degradation in SNR must be considered in wide dynamic range applications.

USING DDS SYSTEMS AS ADC CLOCK DRIVERS
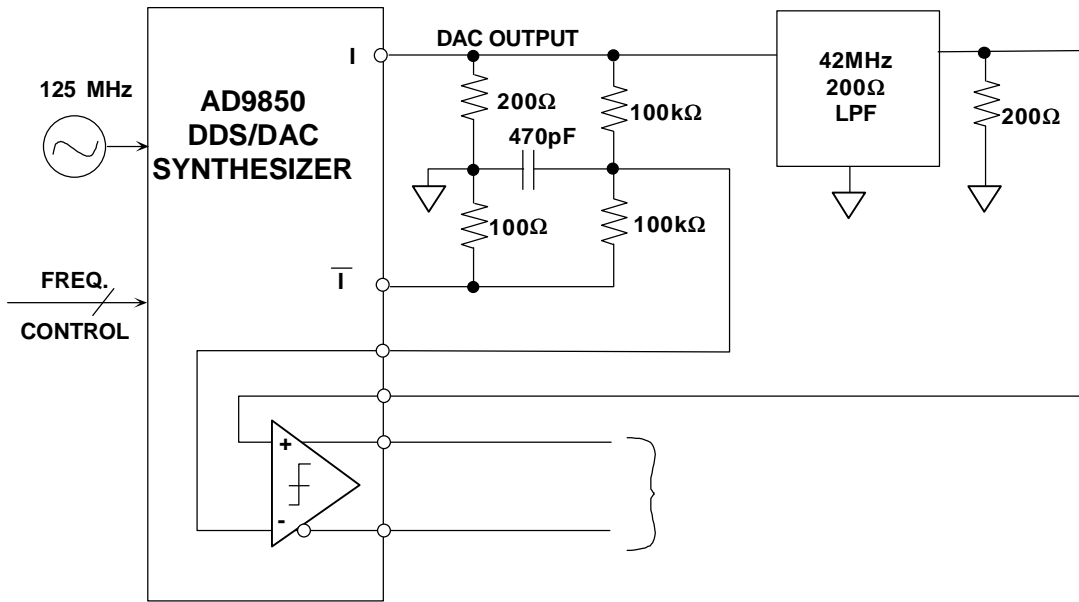
6.8

AMPLITUDE MODULATION IN A DDS SYSTEM

Amplitude modulation in a DDS system can be accomplished by placing a digital multiplier between the lookup table and the DAC input as shown in Figure 6.9. Another method to modulate the DAC output amplitude is to vary the reference voltage to the DAC. In the case of the AD9850, the bandwidth of the internal reference control amplifier is approximately 1MHz. This method is useful for relatively small output amplitude changes as long as the output signal does not exceed the +1V compliance specification.

AMPLITUDE MODULATION IN A DDS SYSTEM

f_C

PHASE ACCUMULATOR

SIN LOOKUP TABLE

N

AM REGISTER

MULTIPLIER

N

DAC

OUTPUT

V_{REF}

ANALOG DEVICES
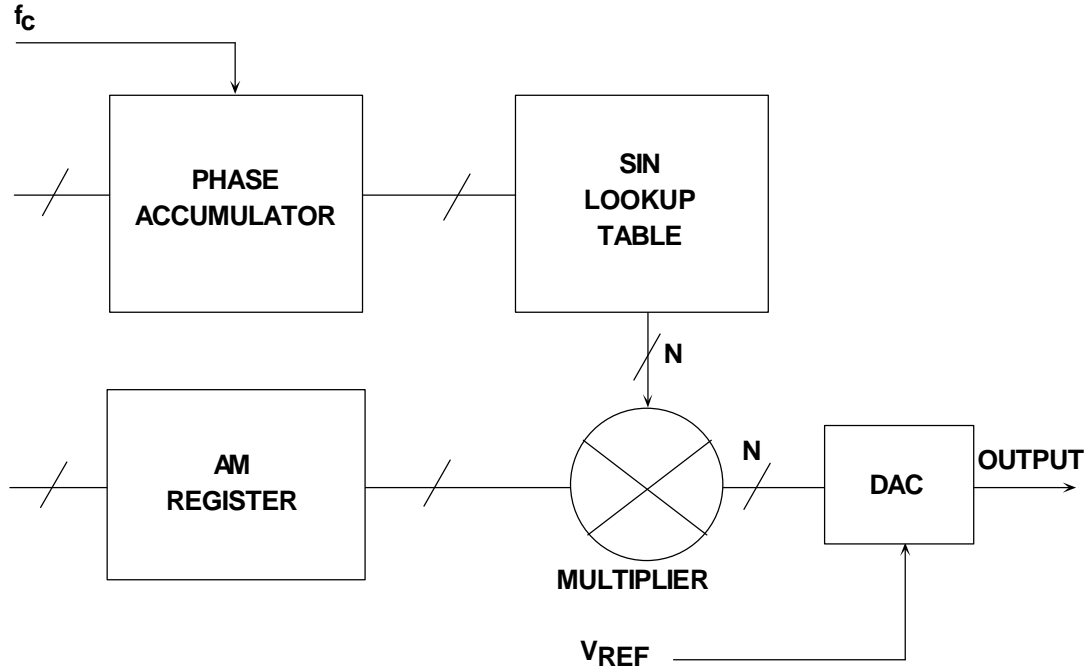
6.9

THE AD9830/9831 COMPLETE DDS SYSTEMS

The AD9830/9831 CMOS DDS systems (see Figure 6.10) contain two frequency registers and four phase registers thereby allowing both frequency and phase modulation. The registers are loaded through a parallel microprocessor port. The DDS chips contain a 32-bit phase accumulator register, 12-bit sin ROM lookup table, and a 10-bit DAC. The AD9830 operates at 50MSPS and dissipates 250mW on the +5V supply. The AD9831 operates at 25MSPS and dissipates 150mW on a +5V supply and 35mW on +3V. Key specifications for the devices are summarized in Figure 6.11.

AD9830/9831, 50/25MSPS COMPLETE DDS SYSTEMS
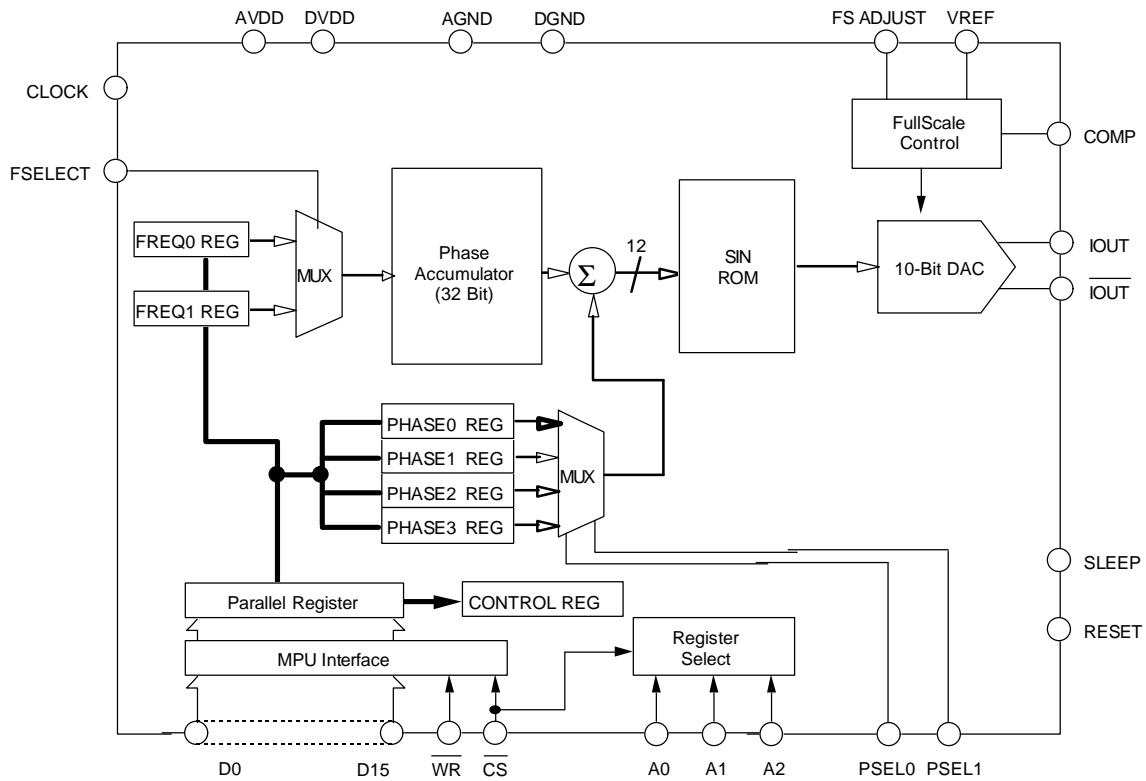
AD9830/9831 DDS SYSTEMS KEY SPECIFICATIONS

- **50MSPS (AD9830), 25MSPS (AD9831) Update Rate**

- **Single +5V (AD9830), +5V/+3V (AD9831) Supply**

- **32-bit Phase Accumulator, 12-bit Address Sine ROM**

- **On Chip 10-bit DAC (70dB SFDR)**

- **Two On-Chip Frequency Modulation Registers**

- **Four On-Chip Phase Modulation Registers**

- **On-Chip Reference**

- **Power Dissipation: 250mW (AD9830),
 150mW (AD9831 @ +5V),   35mW (AD9831 @ +3V)**

- **48-pin TQFP**

SPURIOUS FREE DYNAMIC RANGE CONSIDERATIONS IN DDS SYSTEMS

In many DDS applications, the spectral purity of the DAC output is of primary concern. Unfortunately, the measurement, prediction, and analysis of this performance is complicated by a number of interacting factors.

Even an ideal N-bit DAC will produce harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. This is because the spectral content of the DAC quantization noise varies as this ratio varies, even though its theoretical rms value remains equal to $q/\sqrt{12}$ (where q is the weight of the LSB). The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is simply not true in a DDS system (it is more apt to be a true assumption in an ADC-based system, because the ADC adds a certain amount of noise to the signal which tends to "dither" or randomize the quantization error. However, a certain amount of correlation still exists). For instance, if the DAC output frequency is set to an exact submultiple of the clock frequency, then the quantization noise will be concentrated at multiples of the output frequency, i.e., it is highly signal dependent. If the output frequency is slightly offset, however, the quantization noise will become more random, thereby giving an improvement in the effective SFDR.

This is illustrated in Figure 6.12, where a 4096 point FFT is calculated based on digitally generated data from an ideal 12-bit DAC. In the left-hand diagram, the ratio between the clock frequency and the output frequency was chosen to be exactly 32 (128 cycles of the sinewave in the FFT record length), yielding an SFDR of about 78dBc. In the right-hand diagram, the ratio was changed to 32.25196850394 (127 cycles of the sinewave within the FFT record length), and the effective SFDR is now increased to 92dBc. In this ideal case, we observed a change in SFDR of 14dB just by slightly changing the frequency ratio.
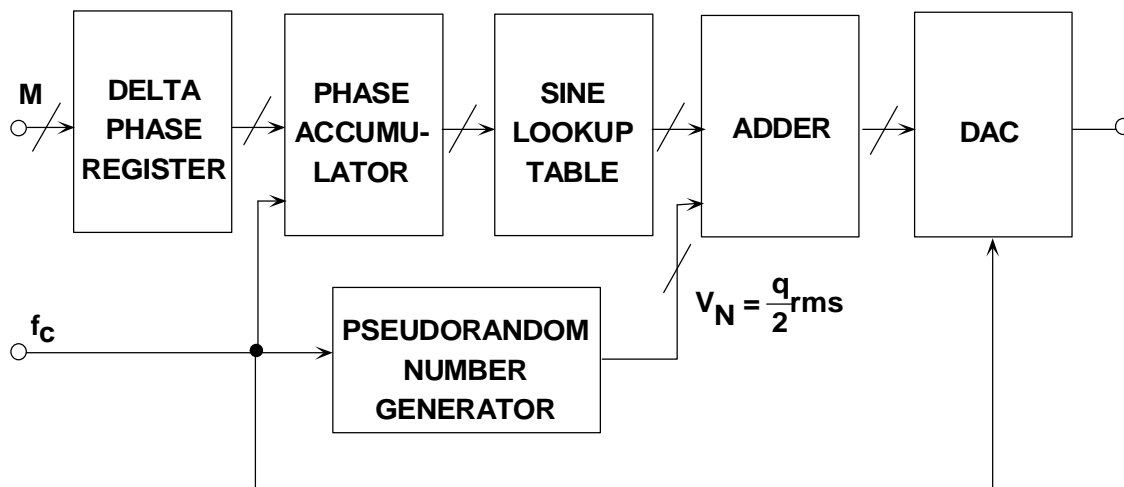
EFFECT OF RATIO OF CLOCK TO OUTPUT FREQUENCY
ON THEORETICAL 12-BIT DAC SFDR USING 4096-POINT FFT

$f_C / f_O = 32$ $f_C / f_O = 32.25196850394$

ANALOG
DEVICES
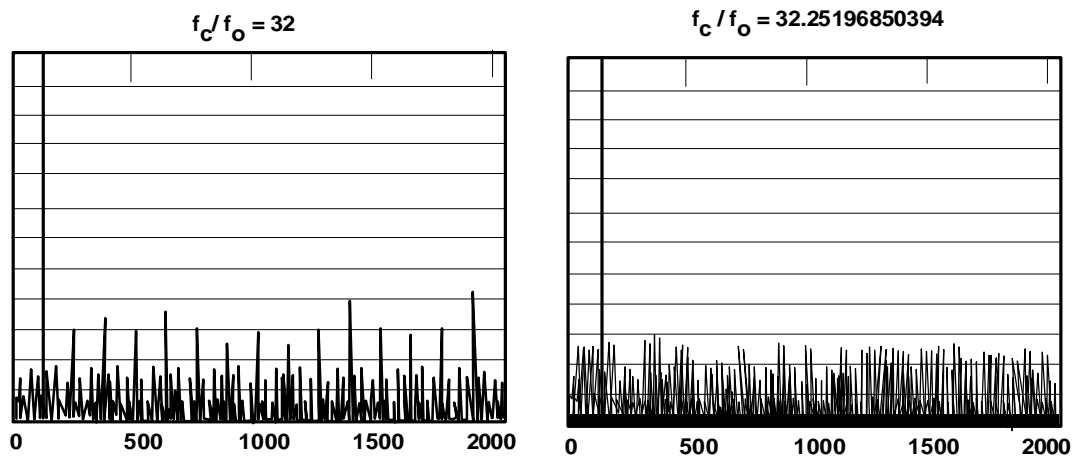
6.12

Best SFDR can therefore be obtained by the careful selection of the clock and output frequencies. However, in some applications, this may not be possible. In ADC-based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system as shown in Figure 6.13 (Reference 5). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about 1/2 LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that dithering is not required.

INJECTION OF DIGITAL DITHER IN A DDS SYSTEM TO RANDOMIZE QUANTIZATION NOISE AND INCREASE SFDR

M — DELTA PHASE REGISTER — PHASE ACCUMU-LATOR — SINE LOOKUP TABLE — ADDER — DAC

f_C — PSEUDORANDOM NUMBER GENERATOR

$$V_N = \frac{q}{2} rms$$

ANALOG DEVICES   **6.13**

A non-ideal DAC will introduce several other mechanisms of distortion. First, the overall integral non-linearity of the DAC transfer function will introduce harmonic distortion. This distortion behaves much like that produced by the non-linearity of an amplifier. The distortion due to the differential non-linearity of the DAC is highly dependent upon the nature of the differential non-linearity and is difficult to predict mathematically. The third source of DAC distortion are code-dependent output glitches. In a DAC there is a transient (or glitch) produced whenever the DAC input code changes. This glitch is usually worst at midscale, where the DAC makes the transition between the codes 1000...000 and 0111...111, and all the DAC bits must switch. These glitches occur because of the unequal turn-on/turn-off times of the DAC current switches. They also occur at 1/4 scale, 1/8 scale, etc., with decreasing amplitude. Because the glitches are code-dependent (hence signal-dependent) they produce harmonics of the fundamental output DAC frequency. For instance, each time the sinewave crosses through mid-scale, a glitch occurs, thereby producing a second harmonic - since the sinewave passes through midscale twice each cycle. The harmonics produced by these code-dependent glitches fold back into the Nyquist bandwidth due to aliasing and thereby affect the SFDR.

CONTRIBUTORS TO DDS DAC DISTORTION

- **Resolution**

- **Integral Non-Linearity**

- **Differential Non-Linearity**

- **Code-Dependent Glitches**

- **Ratio of Clock Frequency to Output Frequency**

14

(Even in an Ideal DAC)

■ **Mathematical Analysis is Difficult !**

Low distortion high-speed DACs generally have a specification for the area of the worst glitch (called *glitch impulse area).* In general, the smaller the glitch area, the better the distortion-but it is difficult to mathematically relate the distortion performance to the glitch area. The glitch impulse area for low distortion DACs is usually less than 30pV-sec. A typical midscale glitch impulse is shown for the AD9721 DAC in Figure 6.15.

AD9720/AD9721 DAC MIDSCALE GLITCH SHOWS 1.34pV-s NET IMPULSE AREA AND SETTLING TIME OF 4.5ns

AD9720

I_{OUT}

100MHz LPF

50Ω

TEST CIRCUIT

5ns/DIVISION
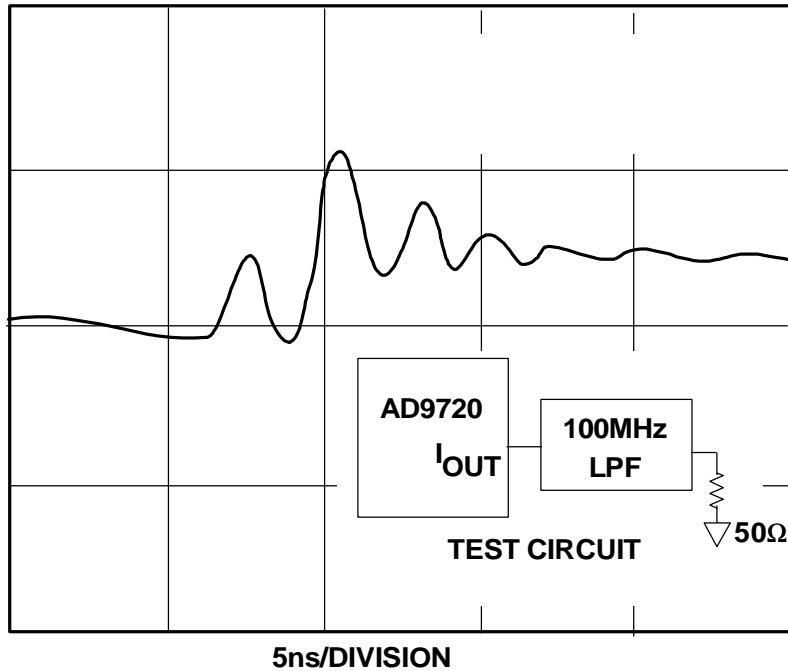
The best way to measure DAC performance is with a spectrum analyzer, with a DDS system used to drive the DAC (Figure 6.16). Because there are nearly an infinite combination of possible clock and output frequencies, SFDR is generally specified for only a few selected combinations. One method is to plot the SFDR as a function of clock frequency for the output frequency slightly offset from 1/3 or 1/4 the clock frequency. The small frequency offset randomizes the quantization noise and also allows the distortion products to be easily observed.

TEST SETUP FOR MEASURING DAC SFDR

**PARALLEL OR
SERIAL PORT**

PC		DDS		LATCH		DAC

N

N

**STABLE
FREQUENCY
REFERENCE**

f_C

f_O

**SPECTRUM
ANALYZER**
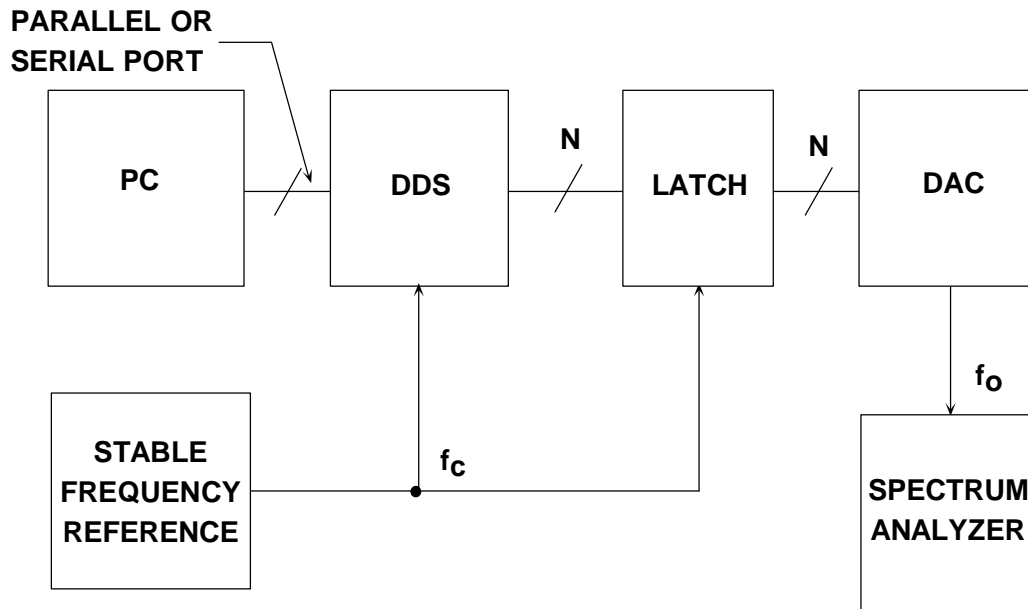
6.16

Note that for the output slightly offset from $f_C/3$, the even harmonics will be aliased very close to the output signal as shown in Figure 6.17. Similarly, for the output slightly offset from $f_C/4$, the odd harmonics will fall close to the output frequency (Figure 6.18). The SFDR at $f_C/3$ is usually considered a worse case condition and is often plotted as a function of clock frequency as shown in Figure 6.19 for the AD9721 10-bit, 100MSPS TTL-compatible DAC.

LOCATION OF EVEN HARMONICS FOR
$f_O = f_C / 3 - \Delta f$

f_O

Δf

10   4   2   8

$\dfrac{f_C}{3}$
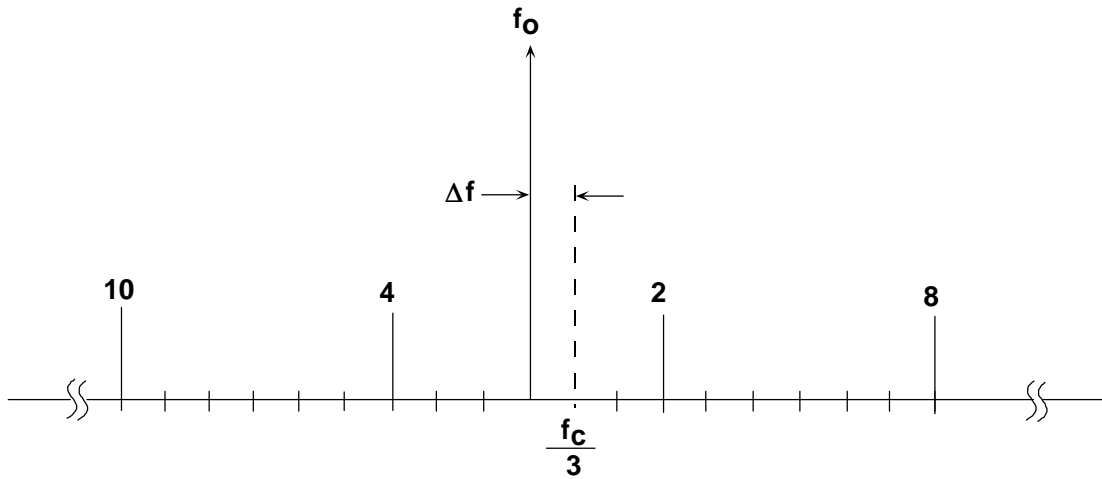
6.17

LOCATION OF ODD HARMONICS FOR
$f_O = f_C / 4 - \Delta f$

f_O

Δf

9   5   3   7

$\dfrac{f_C}{4}$
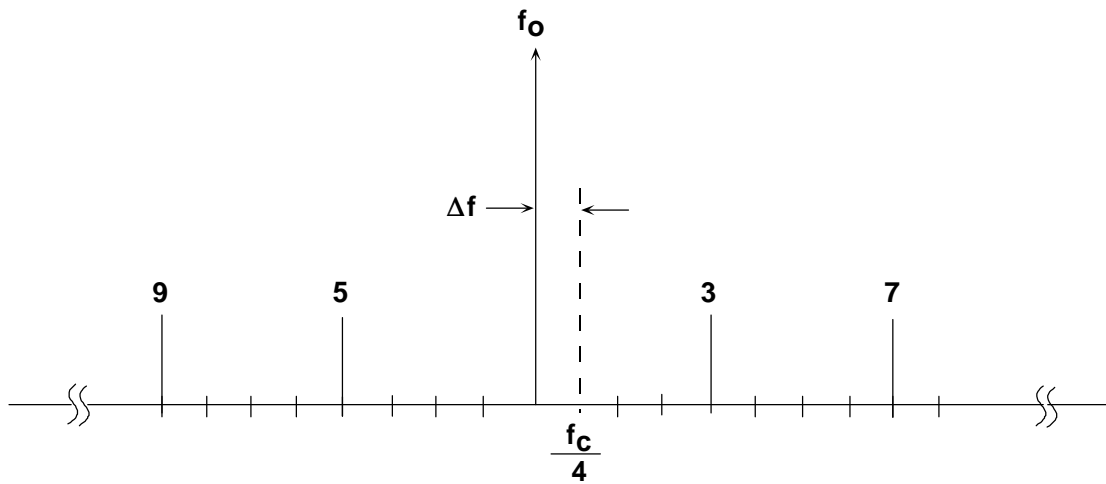
6.18

**SFDR OF AD9721 10-BIT DAC FOR**
$f_O \sim f_C / 3$ (BANDWIDTH: DC TO $f_C / 2$)
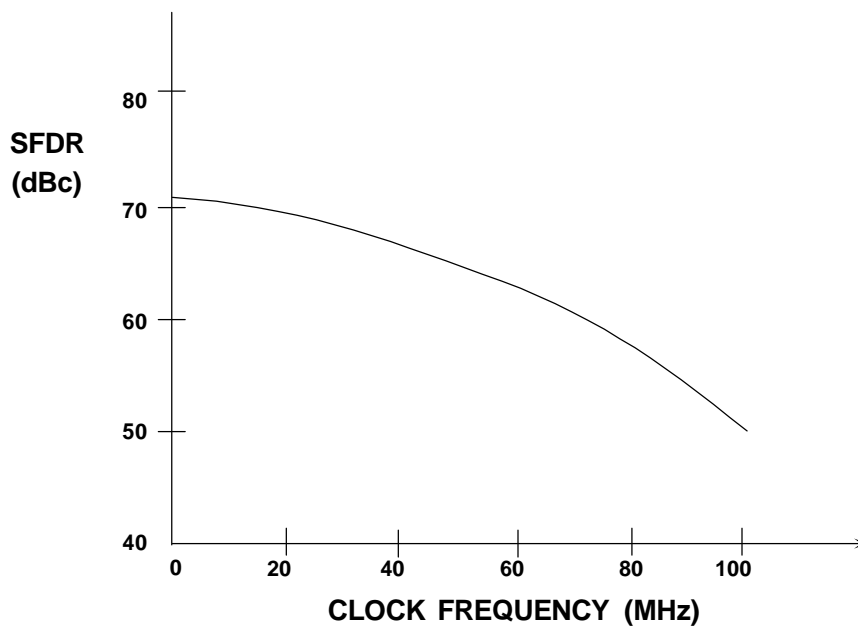
HIGH SPEED LOW DISTORTION DAC ARCHITECTURES

Because of the emphasis in communications systems for DDS DACs with high SFDR, much effort has been placed on determining optimum DAC architectures. Practically all low distortion high speed DACs make use of some form of non-saturating current-mode switching. A straight binary DAC with one current switch per bit produces code-dependent glitches as discussed above and is certainly not the most optimum architecture (Figure 6.20). A DAC with one current source per code level can be shown not to have code-dependent glitches, but it is not practical to implement for high resolutions. However, this performance can be approached by decoding the first few MSBs into a "thermometer" code and have one current switch per level. For example, a 5-bit thermometer DAC would have an architecture similar to that shown in Figure 6.21.

5-BIT BINARY DAC ARCHITECTURES
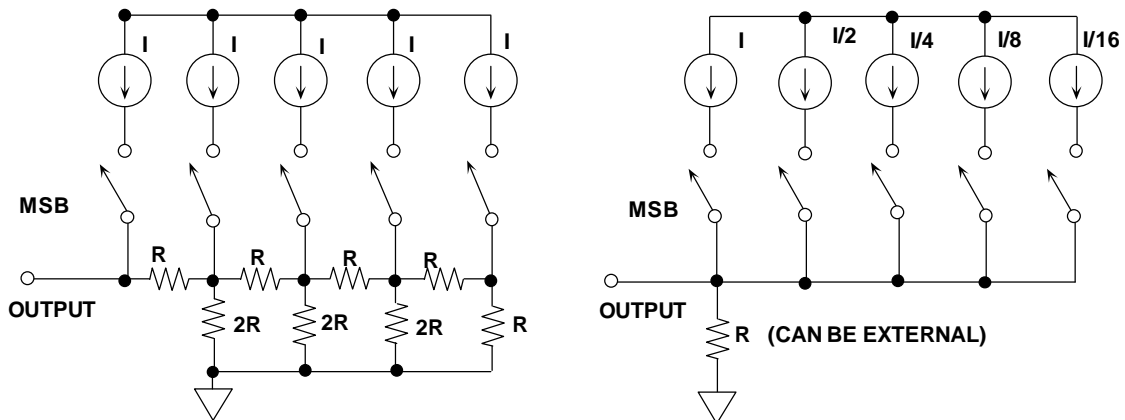
5-BIT "THERMOMETER" OR "FULLY-DECODED" DAC
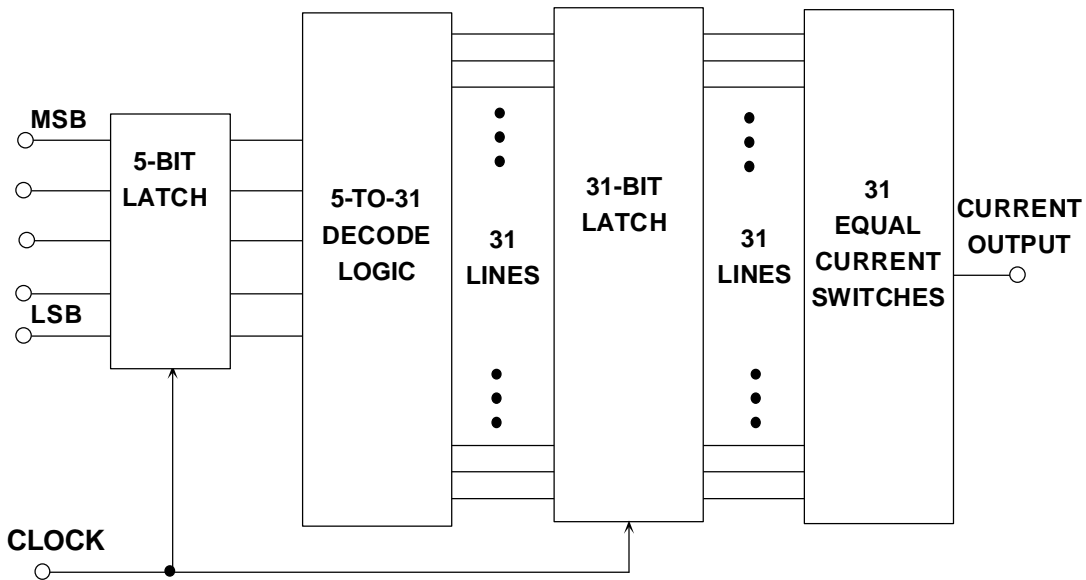
The input binary word is latched and then decoded into 31 outputs which drive a second latch. The output of the second latch drives 31 equally weighted current switches whose outputs are summed together. This scheme effectively removes nearly all the code-dependence of the output glitch. The residual glitch that does occur at the output is equal regardless of the output code change and can be filtered.

The distortion mechanisms associated with the full-decoded architecture are primarily asymmetrical output slewing, finite switch turn-on and turn-off times, and integral nonlinearity.

The obvious disadvantage of this type of thermometer DAC is the large number of latches and switches required to make a 12, 10, or even 8-bit DAC. However, if this technique is used on the 5 MSBs of an 8, 10, or 12-bit DAC, a significant reduction in the code-dependent glitch is possible. This process is called *segmentation* and is quite common in low distortion DACs.

Figure 6.22 shows a scheme whereby the first 5 bits of a 10-bit DAC are decoded as described above and drive 31 equally weighted switches. The last 5 bits are derived from binarily weighted current sources. Equally weighted current sources driving an R/2R resistor ladder could be used to derive the LSBs, however, this approach requires thin film resistors which are not generally available on a low-cost CMOS process. Also, the use of R/2R networks lowers the DAC output impedance, thereby requiring more drive current to develop the same voltage across a fixed load resistance.

10-BIT SEGMENTED DAC

ANALOG
DEVICES
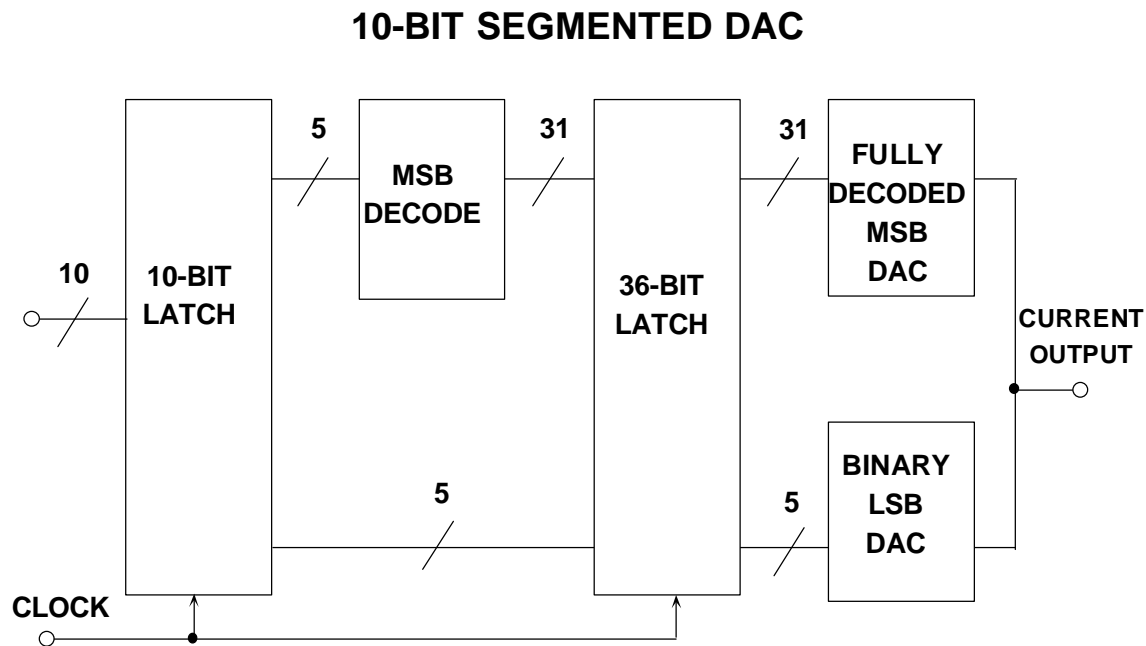
6.22

The AD9850 internal 10-bit DAC uses two major stages of segmentation as shown in Figure 6.23. The first 5 bits (MSBs) are fully decoded and drive 31 equally weighted current switches (320µA each). The next 4 bits are decoded into 15 lines which drive 15 current switches, each supplying 20µA (1/16 the current supplied by each MSB switch). The LSB is latched and drives a single current switch which supplies 10µA (1/32 the current supplied by each MSB switch). A total of 47 current switches and latches are required to implement this architecture.

AD9850 10-BIT CMOS CURRENT SWITCH DAC CORE
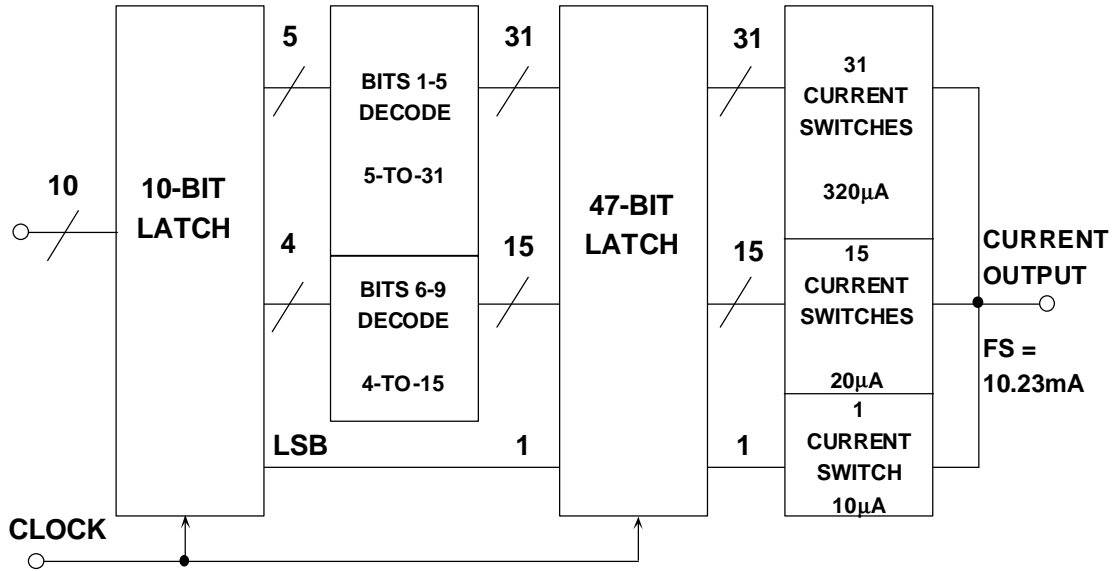
6.23

The basic current switching cell is made up of a differential PMOS transistor pair as shown in Figure 6.24. The differential pairs are driven with low-level logic to minimize switching transients and time skew. The DAC outputs are symmetrical differential currents which help to minimize even-order distortion products (especially which driving a differential output such as a transformer or an op amp differential I/V converter).

The overall architecture of the AD9850 is an excellent tradeoff between power/performance and allows the entire DDS function to be implemented on a standard CMOS process with no thin film resistors. Single-supply operation on +3.3V or +5V makes the device extremely attractive for portable and low power applications. The SFDR performance is typically 60, 55, and 45dBc for output frequencies of 1, 20, and 40MHz, respectively (clock frequency = 125MSPS).

PMOS TRANSISTOR CURRENT SWITCHES
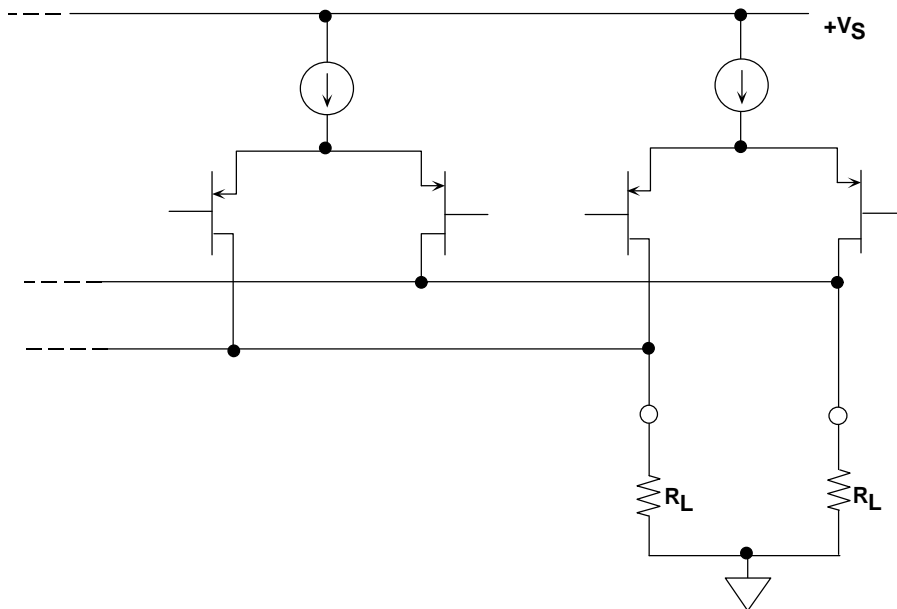
The AD9760 (10-bit), AD9762 (12-bit) and AD9764 (14-bit) 100MSPS DACs utilize the same basic switching core as the AD9850. This family of DACs is pin-compatible, and offers exceptional AC and DC performance. They operate on single +5V or +3V supplies and contain on-chip latches, reference, and are ideal for the transmit channel in wireless basestations, ADSL/HFC modems, and DDS applications. Key specifications for the family are summarized in Figure 6.25.

AD9760/9762/9764 FAMILY OF 100MSPS DACs

■   **Pin-Compatible 10-bit (AD9760), 12-bit (AD9762), and 14-bit (AD9764)**

■   **SFDR for 15MHz Output: -60dBc**

■   **Low Glitch Impulse: 5pVsec**

■   **On-Chip Reference**

■   **Single +5V or +3V Supplies**

■   **Power Dissipation: 175mW @ 5V**

■   **Power-Down Mode: 30mW**

IMPROVING SFDR USING SAMPLE-AND-HOLD DEGLITCHERS

High-speed sample-and-hold amplifiers (such as the AD9100 and AD9101) can be used to deglitch DAC outputs as shown in Figure 6.26. Just prior to latching new data into the DAC, the SHA is put into the *hold* mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the clock frequency and hence are easily filtered. However, great care must be taken so that the relative timing between the SHA clock and the DAC update clock is optimum. In addition, the distortion performance of the SHA must be at least 6 to 10dB better than the DAC, or no improvement in SFDR will be realized. Achieving good results using an external SHA deglitcher becomes increasingly more difficult as clock frequencies approach 100MSPS.

SAMPLE-AND-HOLD (SHA) USED AS DAC DEGLITCHER
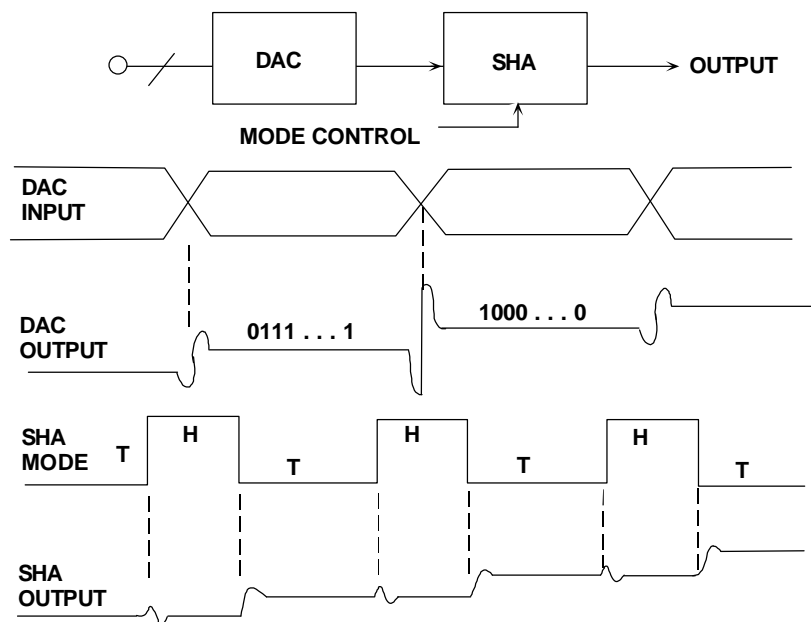
ANALOG DEVICES   6.26

The AD6742 is a 12-bit, 65MSPS low distortion DAC with on-chip SHA deglitcher designed for communications applications. This DAC is fabricated on the XFCB process and provides 75dB SFDR for a 20MHz output. A functional diagram is shown in Figure 6.27, and key specifications in Figure 6.28.

AD6742 12-BIT, 65MSPS DEGLITCHED DAC
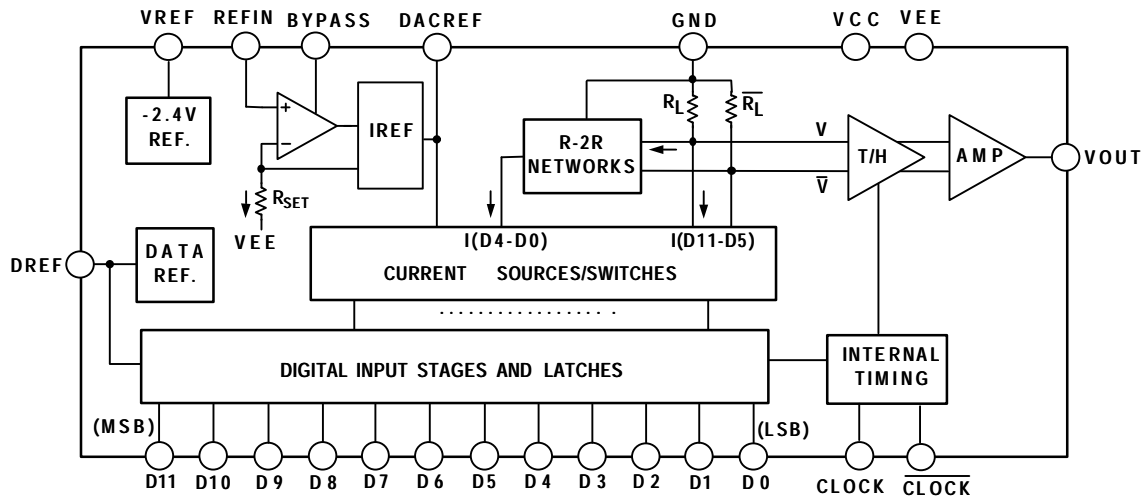
AD6742 12-BIT, 65MSPS DAC KEY SPECIFICATIONS

- ■ **12-bit, 65MSPS Communications DAC**

- ■ **Ideal for Wideband Multichannel Transmit Path**

- ■ **High SFDR: 78dB (typ) @ 20MHz Output, 65MSPS Update**

- ■ **Fabricated on XFCB process**

- ■ **On-Chip Reference**

- ■ **Dual 5V Supplies, 900mW power dissipation**

HIGH SPEED INTERPOLATING DACS

Consider a DDS system which operates at a clock frequency of 100MSPS and outputs a 30MHz sinewave (see Figure 6.29). The first aliased (or image) frequency occurs at 100–30 = 70MHz. Assume we wish the antialiasing filter to attenuate this image frequency component by 60dB. The filter must go from a passband of 30MHz to 60dB stopband attenuation over the transition band lying between 30 and 70MHz (approximately one octave). A Butterworth filter design gives 6dB attenuation per octave for each pole. Therefore, a minimum of 10 poles is required to provide the desired attenuation. Filters become even more complex as the transition band becomes narrower.

LPF REQUIRED TO REJECT IMAGE FREQUENCY
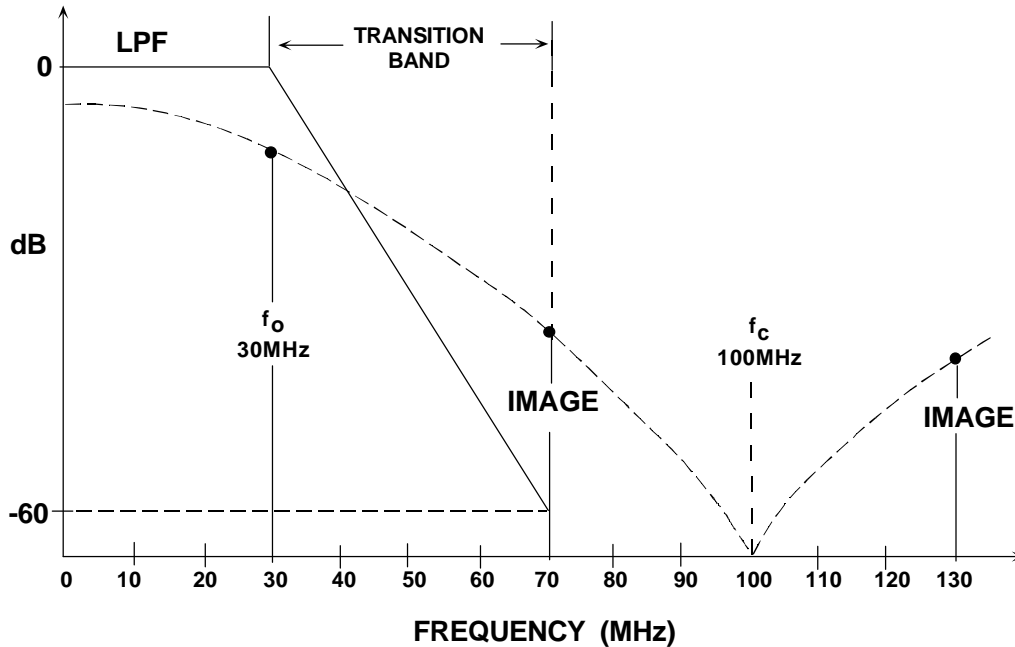
In ADC-based systems, oversampling can ease the requirements on the antialiasing filter, and a sigma-delta ADC has this inherent advantage. In a DAC-based system (such as DDS), the concept of interpolation can be used in a similar manner. This concept is common in digital audio CD players, where the basic update rate of the data from the CD is about 44kSPS. "Zeros" are inserted into the parallel data, thereby increasing the effective update rate to 4-times, 8-times, or 16-times the fundamental throughput rate. The 4x, 8x, or 16x data stream is passed through a digital interpolation filter which generates the extra data points. The high oversampling rate moves the image frequencies higher, thereby allowing a less complex filter with a wider transition band.

The same concept can be applied to a high speed DDS DAC. Assume a traditional DAC is driven at an input word rate of 30MSPS (see Figure 6.30). The maximum realizable DAC output frequency is about 10MHz. The image frequency component at 30–10 = 20MHz must be attenuated by the analog antialiasing filter, and the transition band of the filter is 10 to 20MHz.

Assume that we increase the update rate to 60MSPS by inserting a "zero" between each original data sample. The parallel data stream is now 60MSPS and is passed through the digital interpolation filter which computes the additional data points. The response of the digital filter relative to the 2-times oversampling frequency is shown in Figure 6.30. The analog antialiasing filter transition zone is now 10 to 50MHz (the first image occurs at $2f_C - f_0 = 60-10 = 50$MHz).

f_C = 30MSPS AND f_C = 60MSPS
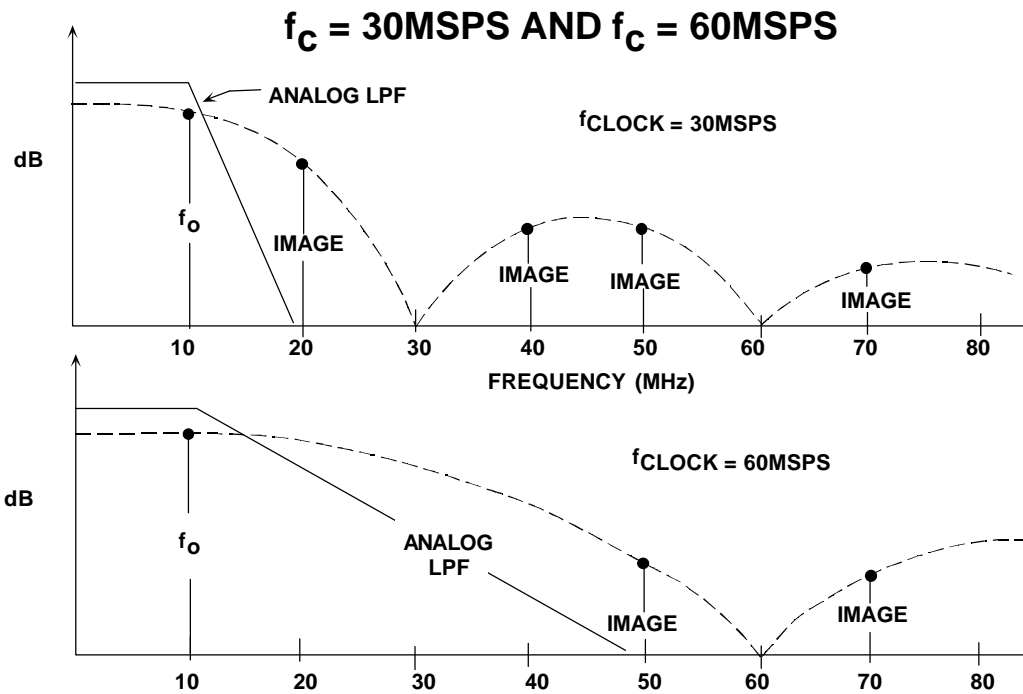
The AD977x is a 4-times oversampling interpolating 10-bit DAC, and a simplified block diagram is shown in Figure 6.31. The device is designed to handle 10-bit input word rates up to about 30MSPS. The internal digital filter consists of a 15-tap filter operating at $2f_C$ followed by a 7-tap filter operating at $4f_C$. The output word rate is 120MSPS, putting the image frequency at $4f_C - f_0 = 120 - 10 = 110$MHz. SFDR of the DAC for a 10MHz output is approximately 60dBc.

INCREASING THE DAC THROUGHPUT RATE BY "K" USING A PLL AND A DIGITAL INTERPOLATION FILTER (INTERPOLATING DAC)
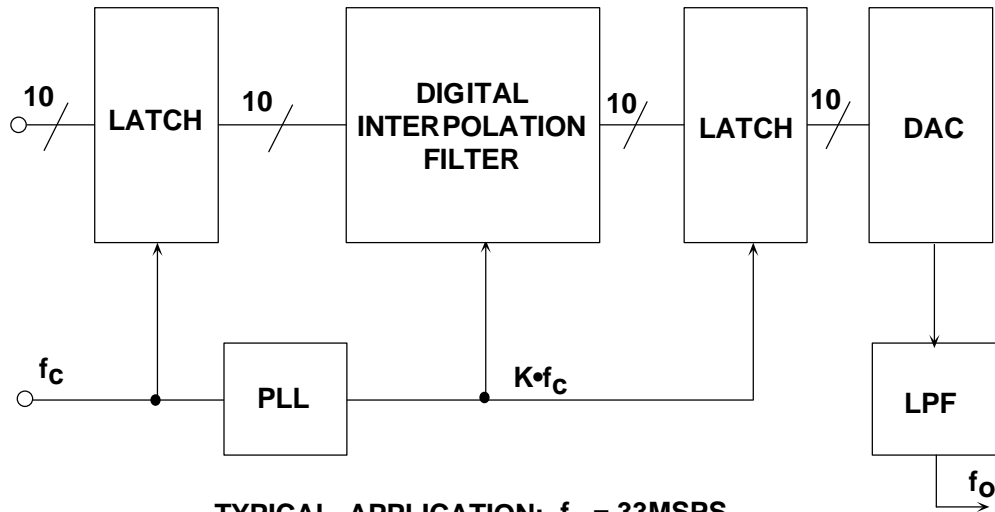
TYPICAL APPLICATION: f_C = 33MSPS
f_O = 10MHz
K = 4 OR 8

ANALOG DEVICES

6.31

# QPSK SIGNAL GENERATION USING DDS (AD9853)

The AD9853 is a digital Quadrature Phase Shift Keying (QPSK) modulator useful in the 5 to 40MHz return path transmitter in a hybrid fiber coax (HFC) CATV cable modem application (see Figure 6.32). This allows asynchronous data transfer over the HFC cable plant. The device takes the serial QPSK data input, splits it into an in-phase (I) and quadrature (Q) signal. The I and Q channel data is then filtered and passed through a digital quadrature modulator. The quadrature modulators are driven by the sine and cosine outputs from the DDS section. The modulator outputs are then recombined digitally and then converted into analog by an internal 10-bit DAC. The resulting QPSK constellation is shown in Figure 6.33. This scheme of modulation is quite common, and results in relatively high noise immunity. Key specifications for the AD9853 are given in Figure 6.34.

AD9853 DIGITAL QPSK MODULATOR
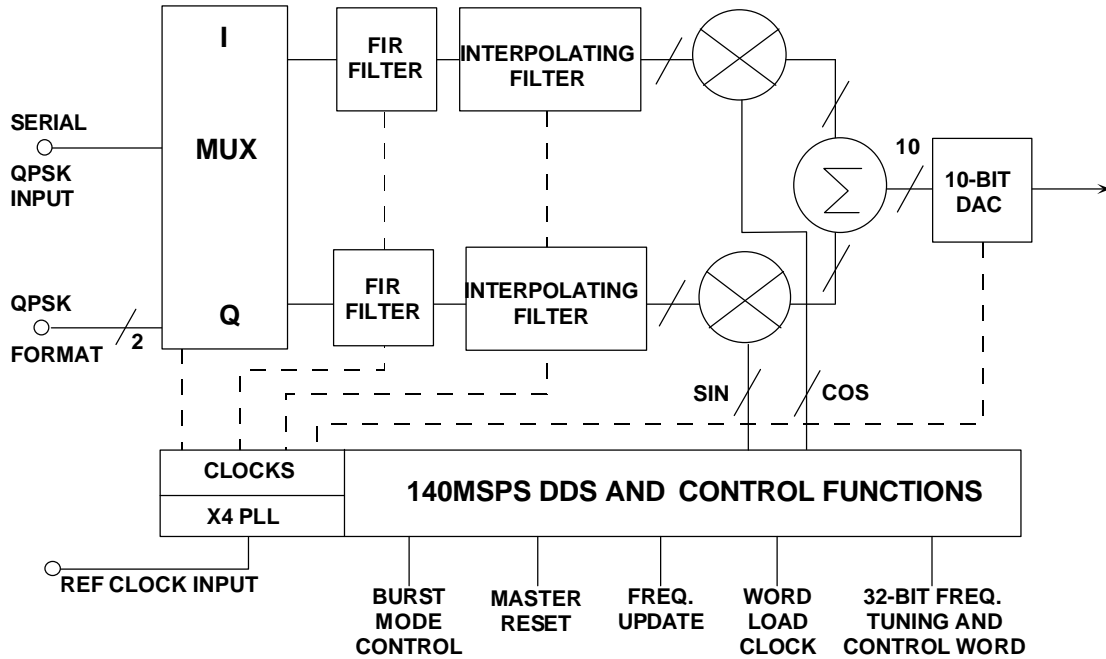
QPSK CONSTELLATION
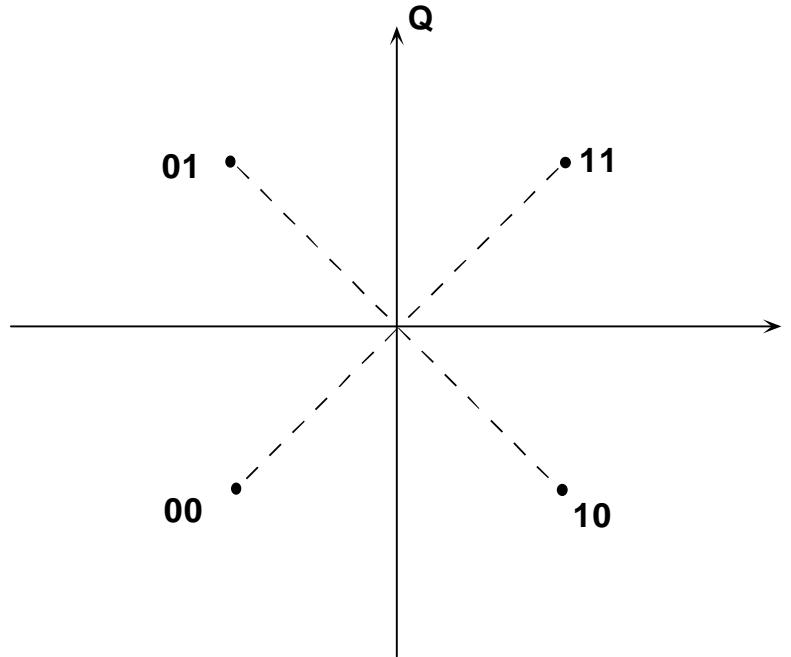
AD9853 DIGITAL QPSK MODULATOR KEY SPECIFICATIONS

■ **Performs Transmit Function for QPSK 5-40MHz Hybrid Fiber Coax (HFC) Return Path**

■ **Includes Raised Cosine Pulse-Shaping Filter (Alpha = 0.5) and Interpolation Filters**

■ **140MSPS Clock Frequency**

■ **46dBc SFDR @ 40MHz Output**

■ **+5V or +3.3V Operation**

■ **300mW Dissipation @ 125MSPS Clock Frequency (30mW Power-Down Mode)**

■ **28-Pin SSOP Surface-Mount Package**

**ANALOG
DEVICES**

6.34

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6.   Henry T. Nicholas, III and Henry Samueli, *An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation*, **IEEE 41st Annual Frequency Control Symposium Digest of Papers**, 1987, pp. 495-502, IEEE Publication No. CH2427-3/87/0000-495.

7.   Henry T. Nicholas, III and Henry Samueli, *The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects*, **IEEE 42nd Annual Frequency Control Symposium Digest of Papers**, 1988, pp. 357-363, IEEE Publication No. CH2588-2/88/0000-357.