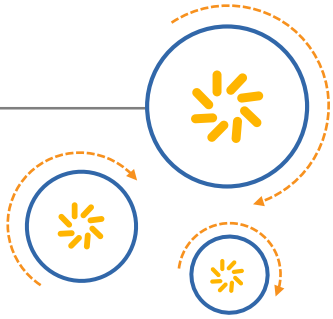
Qualcomm Technologies, Inc.



Qualcomm® Snapdragon™ 410 Processor APQ8016

Device Specification

August 2015

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

LM80-P0436-7 Rev. B

Revision history

Revision	Date	Description
A	May 29, 2015	Initial release
B	August 7, 2015	Added recent changes from source document: ▪ Section 1.3.1 New features integrated into APQ8016 and Table 3-7 Dhrystone and rock bottom power specifications: Updated the frequency information ▪ Table 2-4 Pin descriptions – connectivity functions: Renamed MI2S_1 to Speaker and MI2S_2 to MI2S ▪ Table 2-10 Pin descriptions – general-purpose input/output ports: Updated the type of USB_HS_ID for gpio_110 ▪ Table 3-3 Operating conditions Updated the VDD_PLL2 minimum voltage to 1.72 ▪ Section 3.5 Power sequencing: Corrected the VDD_USBPHY and PLL2 sequence ▪ Section 3.10.5 Serial peripheral interface: Corrected spi frequency to 50Mhz

Contents

Figures

Tables

1 Introduction

This document describes features and functionality of the Qualcomm® Snapdragon™ 410 processor (model APQ8016) for embedded computing.

Qualcomm processors for embedded computing are dedicated to support embedded device OEMs in several ways:

- Longevity beyond lifecycle of mobile chipsets through 2020
- Detailed documentation for developers
- Availability of development kits/community board for early access
- Multiple OS support including mainline Linux support
- Availability of several computing module partners for customization for your individual projects/products

Snapdragon 410 processors deliver high-performance computing, low power consumption and a rich multimedia experience for embedded devices.

It is an ideal solution for any application requiring computing horsepower and integrated WiFi/Bluetooth connectivity: Smart Home; Industrial Appliances, Digital Media and TV dongles, Smart Surveillance and Robotics.

Snapdragon supports a clear deployment path for embedded device OEMs and developers – starting with single-board computers and development kits and scaling up to customer solutions, integration services and production-ready, customizable computing modules.

1.1 Documentation overview

Technical information for the APQ8016 device is primarily covered by the documents listed in Table 1-1. All documents should be studied for a thorough understanding of the device and its applications.

NOTE: This current version is an early release to support initial product developers. The content is subject to change without advance notice.

Table 1-1 Primary APQ8016 documentation

Document number	Title and description
LM80-P0436-7 (this document)	*Qualcomm® Snapdragon™ 410 Processor APQ8016 Device Specification* Provides all APQ8016 electrical specifications and mechanical information. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
LM80-P0436-6	*Qualcomm® Snapdragon™ 410 Processor APQ8016 GPIO Pin Assignments* A Microsoft Excel spreadsheet listing all APQ8016 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations. This can be used to help designers define their products' GPIO assignments.

This document is organized as follows:

Chapter 1 Provides an overview of the APQ8016 documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum ratings and operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of the APQ8016.

Chapter 6 Presents procedures and specifications for mounting the APQ8016 onto printed circuit boards (PCBs).

Chapter 7 Presents APQ8016 reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 APQ8016 introduction

Embedded computing devices continue to integrate more and increasingly complex functions, and support more functionality while maintaining performance, board space, and cost.

These demands are met by the APQ8016 (Figure 1-1) – with its ARM Cortex-A53 application processors – which further expand mass-market chipset capabilities by making rich multimedia features accessible to more consumers worldwide.

The APQ8016 has a high level of integration that reduces the bill-of-material (BOM), which delivers board-area savings. The cost and time-to-market advantages of this IC will help drive adoption in mass markets around the world.

Wireless products based on the APQ8016 chipset may include:

- Music player-enabled devices and applications
- Cameras
- Devices with gaming, streaming video, and video conferencing features
- GPS, GLONASS, and BeiDou for global location-based service (with WGR7640).
- Wireless connectivity–Bluetooth, WLAN, and FM receiver (with WCN3620)

The APQ8016 benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated application processors and hardware cores to eliminate multimedia coprocessors, and to provide superior image quality and resolution for devices while extending application times
  - Higher computing power for high-end applications, and DC power savings for longer run times
- Position location and navigation systems supported through the WGR7640 global navigation satellite system (GNSS) receiver
  - The APQ8016 Chipset supports Gen 8C operation
  - Standalone GPS, GLONASS, and COMPASS
  - 1 Hz tracking
  - Small, power- and thermal-efficient WGR7640 packaging
- A single platform providing dedicated support for all market-leading codecs and other multimedia formats to support deployments around the world
- DC power reduction using innovative techniques
- Support for the latest, most popular operating systems

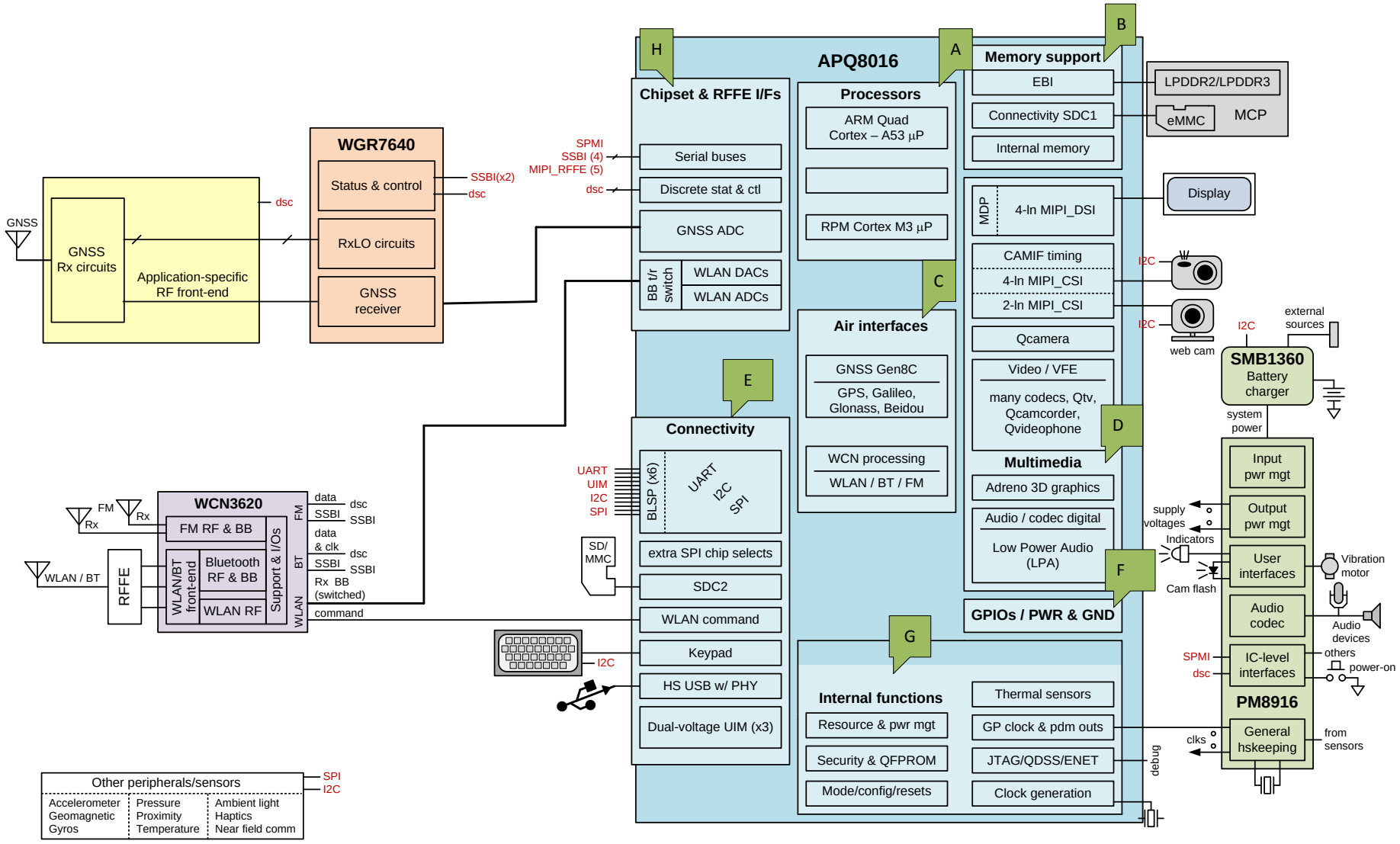


Figure 1-1 APQ8016 functional block diagram and example application

The APQ8016 is fabricated using the advanced 28 nm LP CMOS process, and is available in the 760 NSP; a 14.0 ×12.0 × 0.96 mm package with many ground pins for improved electrical grounding, mechanical strength, and thermal conductivity. See Chapter 2 for pin assignment details and Chapter 4 for mechanical information.

The APQ8016 supports high-performance applications worldwide using GPS, GNSS, and BeiDou wireless networks.

Complementary ICs within the APQ8016 chipset include:

- GPS IC: WGR7640 is a GNSS receiver input for GPS, GLONASS, and COMPASS operation
- Power management: PM8916
- Wireless connectivity: WCN3620 for WLAN, Bluetooth, and FM

The APQ8016 chipset and system software solution supports the Convergence Platform for applications by leveraging the years of systems expertise and field experience with GNSS technologies.

Since the APQ8016 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the APQ8016 document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within its functional block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

1.2.1 Device variants

Information about device variants will be provided in future revisions of this document.

1.3 APQ8016 features

NOTE: Some of the hardware features integrated within the APQ8016 must be enabled by software. Refer to the latest version of the applicable software release notes to identify the enabled APQ8016 features.

1.3.1 Features integrated into APQ8016

Features integrated into APQ8016 are as follows:

- Designed up to 1.2 GHz Quad ARM Cortex-A53 64-bit application processors with 512 kB L2 cache
- 28 nm LP process for lower active power dissipation, and faster peak CPU performance
- Single-channel, non-PoP high-speed memory – LPDDR2/LPDDR3 SDRAM up to 533 MHz clock rate
- QDSP6 v5 processor (vocoder) up to 691 MHz
- Three dual-voltage UIM ports
- Qualcomm Adreno™ A306 3D graphics core

1.3.2 Summary of APQ8016 features

APQ8016 features are summarized in Table 1-2.

Table 1-2 Summary of APQ8016 features

Feature	APQ8016 capability
A ***Processors***	
Applications	ARM Cortex-A53 microprocessor cores up to 1.2 GHz ▪ 64-bit processor ▪ Quad core, 512 kB L2 cache ▪ Primary boot processor
RPM system	▪ Cortex M3: Modem power manager (MPM) ▪ MPM coordinates shutdown/wakeup, clock rates, and VDDs
B ***Memory support***	
System memory via EBI	Non PoP LPDDR2, LPDDR3 SDRAM; 32-bit wide; up to 533 MHz
Graphics internal memory	128 kB unified SRAM pool on-chip memory (GMEM)
External memory via SDC1	eMMC v4.5/SD flash devices
C ***RF Support***	
Air interfaces ▪ WLAN/BT/FM	 ▪ Yes – all (with WCN3620)
GNSS – Qualcomm IZat™ location engine	Gen 8C: Support for 3 bands ***concurrently***: ▪ GPS, BeiDou, and Glonass or ▪ GPS, BeiDou, and Galileo
D ***Multimedia***	
Display interfaces ▪ MIPI_DSI ▪ General display features	▪ HD (1280 x 720) 60 fps; 16/18/24 bpp RGB ▪ MIPI DSI 4-lane ▪ Wifi display – 720p 30/1080p 30 ▪ FHD + 720p external wireless display

Feature	APQ8016 capability
Camera interfaces ▪ Number of CSIs ▪ Primary (CSI0) ▪ Secondary (CSI1) ▪ Configurations supported ▪ General camera features	▪ Qcamera ▪ Two; 1.5 Gbps per lane ▪ 4-lane; supports CMOS and CCD sensors ▪ Up to 13 MP sensors ▪ 2-lane MIPI_CSI – webcam support up to 8 MP sensors ▪ Pixel manipulations, camera modes, image effects, and post-processing techniques, including defective pixel correction ▪ I^2C control
Mobile display processor	MDP for display processing
Video applications performance ▪ Encode ▪ Decode	 ▪ 720p 30 fps (H.264 Baseline/MPEG-4) ▪ 30 fps 1080p (MPEG-4/H.264/VP8/H.263) ▫ WFD 720p @ 30 fps ▪ 30 fps 1080p (MPEG-4/H.264/H.263/DivX/MPEG2/VC1/Soreson/VP8) ▪ WFD 1080p @ 30 fps
Graphics	Adreno 306; up to 400 MHz 3D graphics accelerator
Audio ▪ Low-power audio ▪ Voice codec support ▪ Audio codec support ▪ Enhanced audio ▪ Synthesizer	 ▪ Low power audio for mp3 and AAC playback; surround sound; ▪ Versatile – many audio playback and voice modes; encoders for audio and FM ▪ recording; many concurrency modes ▪ G711; Raw PCM; QCELP; EVRC, -B, -WB; AMR-NB, -WB; GSM-EFR, ▪ -FR, -HR ▪ MP3; AAC, +, eAAC; AMR-NB, -WB, G.711, WMA 9/10 Pro ▪ Dolby Digital Plus and DTS-HD surround sound ▪ Fluence™ Noise Cancellation ▪ QAudioFX/Qconcert/QEnsemble ▪ 128-voice polyphony wavetable
Web technologies	▪ V8 JavaScript Engine optimizations ▪ Webkit browser JPEG hardware decode acceleration ▪ Networking Stack IP and HTTP tuning ▪ Flash 10.x and video processor decode optimization
E ***Connectivity***	
BLSP ports ▪ UART ▪ I^2C ▪ SPI (master only)	6, 4-bits each; multiplexed serial interface functions ▪ Yes – up to 4 Mbps ▪ Yes – cameras, sensors, SMB, etc. ▪ Yes – cameras, sensors, etc.
UIM	Three ports – dual voltage (1.8 V/2.85 V)
USB	One USB 2.0 high-speed
Secure digital interfaces	▪ Up to two ports, both dual-voltage ▪ One 8-bit and one 4-bit ▪ SD 3.0; SD/MMC card; eMMC v4.5
Wireless connectivity ▪ WLAN ▪ Bluetooth ▪ FM radio	▪ With WCN3620 ▪ 802.11 a/b/g/n ▪ BT 4.0 LE and earlier ▪ Rx

Feature	APQ8016 capability
Touch screen support	Capacitive panels via external IC (I^2C, SPI, and interrupts)
Audio interfaces ▪ DMIC ▪ MI^{2}S ▪ CDC PDM port	 ▪ One port for digital microphone application ▪ Up to two ports (primary and secondary ports) ▪ Interface between PM8916 and APQ8016 for audio application
F ***Configurable GPIOs***	
Number of GPIO ports	122 GPIOs – GPIO_0 to GPIO_121
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	The logic block used for configuring different IOs and interfaces for the desired functionality and pad attributes
G ***Internal functions***	
PLLs and clocks	▪ Multiple clock regimes; watchdog and sleep timers ▪ 19.2 MHz CXO master clock input ▪ General-purpose outputs: M/N counter, PDM
Resource and power manager	▪ Fundamental to power management ▪ Key blocks: RPM core, Cortex M3, security controller, MPM ▪ Improved efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes
Debug	JTAG, QDSS
Others	Thermal sensors; modes and resets; peripheral subsystem
H ***Chipset and RF front-end (RFFE) interface features***	
RFICs ▪ GNSS baseband data ▪ Status and control	▪ WGR7640 ▪ Rx analog interface ▪ SSBIs and discrete signals as needed via GPIOs
Power management	▪ PM8916 ▪ 2-line SPMI; dedicated clock and reset lines; plus other GPIOs as needed
WCN wireless connectivity ▪ WLAN baseband data ▪ WLAN status and control ▪ Bluetooth ▪ FM radio	▪ WCN3620 ▪ Multiplexed Rx/Tx analog interface ▪ Proprietary 5-line interface ▪ 2-line data interface plus SSBI ▪ 1-line data interface plus SSBI[1]
QCA near field communicator	I^2C plus other GPIOs as needed
Fabrication technology and package	
Digital die	28 nm LP CMOS
Small, thermally efficient package	760 NSP: 14.0 × 12.0 × 0.96 mm; 0.4 mm pitch

[1] Currently not supported in DragonBoard 410c software

1.4 Terms and acronyms

Table 1-3 defines terms and acronyms commonly used throughout this document.

Table 1-3 Terms and acronyms

Term	Definition
3GPP	3rd Generation Partnership Project
ADC	Analog-to-digital converter
AFR	Average failure rate
BAM	Bus Access Manager
APC	Application microprocessors
AR	Area ratio
BLSP	BAM Low-Speed Peripheral
bps	Bits per second
BT	Bluetooth
CSI	Camera serial interface
CTS	Clear to Send
DAC	Digital-to-analog converter
DDR	Double data rate
DSI	Display serial interface
EBI	External bus interface
GLONASS	Global orbiting navigation satellite system
GMEM	Graphics internal memory
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPS	Global positioning system
I^2C	Inter-integrated circuit
I^2S	Inter-IC sound
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1760)

Term	Definition
kbps	kilobits per second
LCD	Liquid crystal display
LPA	Low-power audio
LSB	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MDP	Mobile display processor
MIPI	Mobile industry processor interface
MMC	Multimedia card
MPM	Modem power management
MSB	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
MSL	Moisture-sensitivity level
NSMD	Non-solder-mask-defined
NSP	Nanoscale package
PDM	Pulse-density modulation
PM	Power management
QDSS	Qualcomm debug subsystem
QFPROM	Qualcomm fuse programmable read-only memory
QTI	Qualcomm Technologies, Inc.
QUP	Qualcomm unified peripheral
RPM	Resource power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SEE	Qualcomm Secure Execution Environment
SFS	Secure file system
SIM	Subscriber identity module
SMT	Surface mount technology

Term	Definition
SPI	Serial peripheral interface
SPMI	System power management interface
SSBI	Single-wire SBI
UART	Universal asynchronous receiver/transmitter
UIM	User identification module
USB	Universal serial bus
VDD	Supply voltage
VREF	Reference voltage
VREG	Voltage regulation
WCN	Wireless connectivity network
WLAN	Wireless local area network
XO	Crystal oscillator

1.5 Special marks

Table 1-4 defines special marks used in this document.

Table 1-4 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The APQ8016 is available in the 760 NSP – see Chapter 4 for package details. A high-level view of all pin assignments is shown in Figure 2-2. The pins are colored to indicate which function type they support, as defined in Figure 2-1.

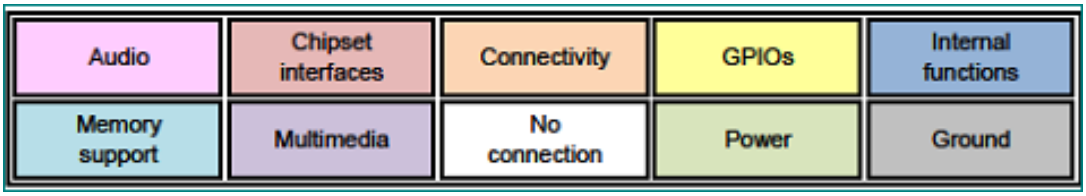


Figure 2-1 APQ8016 pin assignments – legend

The text within Figure 2-2 is difficult to read when viewing an 8½" by 11" hard copy. These other viewing options are available:

- Print that one page on a 11" by 17" sheet.
- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *DragonBoard 410c based on Qualcomm Snapdragon 410 processor GPIO Pin Assignment Spreadsheet* (LM80-P0436-6). This Microsoft Excel spreadsheet lists all APQ8016 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

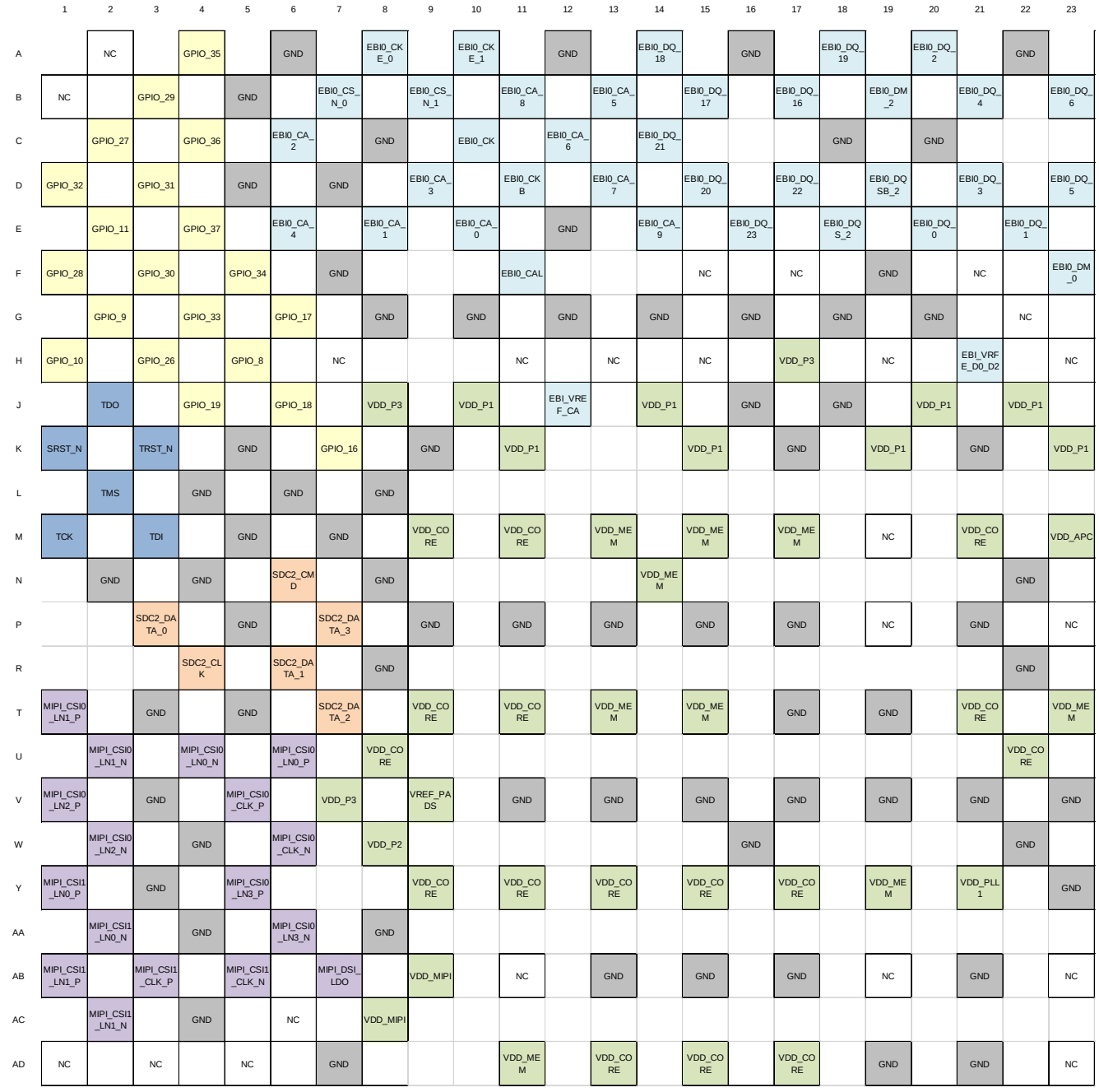


Figure 2-2 High-level view of APQ8016 pin assignments (top view)

2.1 BAM-enabled low-speed peripheral (BLSP)

The BAM integrates three serial bus cores: UARTDM, SPI, and I^{2}C. The SPI and I^{2}C cores are, in turn, integrated into a single core called the Qualcomm Unified Peripheral (QUP) where both the sub-cores share the same FIFO. The UARTDM is integrated separately with its own FIFO. All the cores share the same bus interface.

The external I/O ports of these cores are shared and only one of the cores can be used at any given time. However, in the mode where UARTDM is used as a two pin UART interface, the I^{2}C, which is also a two pin interface, can be used simultaneously with UART functionality.

The BLSP supports the following serial protocols:

- UART_DM
  - Up to 4 Mbps UART
  - Supports all baud rates from 75 to 115200 bps and 4 Mbps
  - 5-8 bits character size, 0.5-2 bits stop bit, no/even/odd/space parity
  - Optional HW flow control based on CTS/RFR (HW or SW based)
  - Other: RX-break, hunt char, sticky error status, overflow detection, FIFO watermarking, FIFO resizing, HW data timeout, HW inactivity timeout
- I^{2}C (master only), driven by QUP
  - Up to 3.4 MHz clock rate
  - For timing spec and protocol features, refer to section 3.10.4
- SPI, driven by QUP
  - Up to 50 MHz operation on all six possible ports
  - For timing spec information, refer to section 3.10.6

The following limitations apply to all six BLSPs:

- The UART controller is muxed behind BLSP1 and BLSP 2. As a result, only BLSP1 and BLSP2 can be configured for UART.
- I^{2}C and SPI cannot be used at the same time on the same BLSP (since they share the QUP controller)
- Two 2-pin UART interfaces cannot be used together on the same BLSP interface
- Two I^{2}C interfaces cannot be used simultaneously through the same BLSP interface

Detailed pin assignments are presented in Table 2-1 and Table 2-2.

Table 2-1 BLSP alternate function configurations

Pad name	Alternate functions		
GPIO[0]	BLSP1_SPI_MOSI	BLSP1_UART_TX	
GPIO[1]	BLSP1_SPI_MISO	BLSP1_UART_RX	
GPIO[2]	BLSP1_SPI_CS_N	BLSP1_UART_CTS_N	BLSP1_I2C_SDA_A

Pad name	Alternate functions		
GPIO[3]	BLSP1_SPI_CLK	BLSP1_UART_RFR_N	BLSP1_I2C_SCL_A
GPIO[4]	BLSP2_SPI_MOSI	BLSP2_UART_TX	
GPIO[5]	BLSP2_SPI_MISO	BLSP2_UART_RX	
GPIO[6]	BLSP2_SPI_CS_N	BLSP2_UART_CTS_N	BLSP2_I2C_SDA_A
GPIO[7]	BLSP2_SPI_CLK	BLSP2_UART_RFR_N	BLSP2_I2C_SCL_A
GPIO[8]	BLSP3_SPI_MOSI		
GPIO[9]	BLSP3_SPI_MISO		
GPIO[10]	BLSP3_SPI_CS_N		BLSP3_I2C_SDA_A
GPIO[11]	BLSP3_SPI_CLK		BLSP2_I2C_SCL_A
GPIO[12]	BLSP4_SPI_MOSI		
GPIO[13	BLSP4_SPI_MISO		
GPIO[14]	BLSP4_SPI_CS_N		BLSP4_I2C_SDA_A
GPIO[15]	BLSP4_SPI_CLK		BLSP4_I2C_SCL_A
GPIO[16]	BLSP5_SPI_MOSI		
GPIO[17]	BLSP5_SPI_MISO		
GPIO[18]	BLSP5_SPI_CS_N		BLSP5_I2C_SDA_B
GPIO[19]	BLSP5_SPI_CLK		BLSP5_I2C_SCL_B
GPIO[20]	BLSP6_SPI_MOSI		
GPIO[21]	BLSP6_SPI_MISO		
GPIO[22]	BLSP6_SPI_CS_N		BLSP6_I2C_SDA_A
GPIO[23]	BLSP6_SPI_CLK		BLSP6_I2C_SCL_A

Table 2-2 BLSP internal pin mapping

Pin	4-pin UART	I2C + GPIOs	I2C + 2-pin UART	4-pin SPI	4 GPIOs
3	UART_TX_DATA	GPIO_XX	UART_TX_DATA	SPI_MOSI_DATA	GPIO_XX
2	UART_RX_DATA	GPIO_XX	UART_RX_DATA	SPI_MISO_DATA	GPIO_XX
1	UART_CTS_N	I2C_DATA	I2C_DATA	SPI_CS_N	GPIO_XX
0	UART_RFR_N	I2C_CLK	I2C_CLK	I2C_CLK	GPIO_XX

2.2 I/O parameter definitions

Table 2-3 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: ■ NP: pdpukp = default no-pull with programmable options following the colon (:) ■ PD: nppukp = default pull-down with programmable options following the colon (:) ■ PU: nppdkp = default pull-up with programmable options following the colon (:) ■ KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
P1	EBI Pad group 1 (EBI for LPDDR2/LPDDR3 memory); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P4	Pad group 4 (UIM3); tied to VDD_P4 pins (1.8 V or 2.95 V)

Symbol	Description
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.2 V or 1.8 V)
MIPI	Supply voltage for MIPI_CSI, MIPI_DSI circuits, and I/Os; tied VDD_MIPI (1.8 V only)
Output current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated; additional details will be given in future revisions of this document.
SDIO2 pads	Programmable drive strength, 2 to 8 mA in 2 mA steps
Others[1]	Programmable drive strength, 2 to 16 mA in 2 mA steps

[1] Digital pads other than EBI pads or high-voltage tolerant pads.

2.2.1 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-4: Memory support functions

Table 2-5: Multimedia functions

Table 2-6 Connectivity functions

Table 2-7: Internal functions

Table 2-9: Chipset interface functions

Table 2-10: General-purpose input/output ports

Table 2-11: No connection, do not connect, and reserved pins

Table 2-12: Power supply pins

Table 2-13: Ground pins

Table 2-4 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
E10	EBI_CA_0		P1	DO	LPDDR2/LPDDR3 command/address bit 0
E8	EBI_CA_1		P1	DO	LPDDR2/LPDDR3 command/address bit 1
C6	EBI_CA_2		P1	DO	LPDDR2/LPDDR3 command/address bit 2
D9	EBI_CA_3		P1	DO	LPDDR2/LPDDR3 command/address bit 3

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
E6	EBI_CA_4		P1	DO	LPDDR2/LPDDR3 command/address bit 4
B13	EBI_CA_5		P1	DO	LPDDR2/LPDDR3 command/address bit 5
C12	EBI_CA_6		P1	DO	LPDDR2/LPDDR3 command/address bit 6
D13	EBI_CA_7		P1	DO	LPDDR2/LPDDR3 command/address bit 7
B11	EBI_CA_8		P1	DO	LPDDR2/LPDDR3 command/address bit 8
E14	EBI_CA_9		P1	DO	LPDDR2/LPDDR3 command/address bit 9
F11	EBI_CAL_REXT		–	AI	LPDDR2/LPDDR3 calibration resistor
C10	EBI_CK		P1	DO	LPDDR2/LPDDR3 differential clock (+)
D11	EBI_CKB		P1	DO	LPDDR2/LPDDR3 differential clock (-)
A8	EBI_CKE_0		P1	DO	LPDDR2/LPDDR3 clock enable 0
A10	EBI_CKE_1		P1	DO	LPDDR2/LPDDR3 clock enable 1
B7	EBI_CS0_N		P1	DO	LPDDR2/LPDDR3 chip select 0
B9	EBI_CS1_N		P1	DO	LPDDR2/LPDDR3 chip select 1
F23	EBI_DM_0		P1	DO	LPDDR2/LPDDR3 data mask for byte 0
E24	EBI_DM_1		P1	DO	LPDDR2/LPDDR3 data mask for byte 1
B19	EBI_DM_2		P1	DO	LPDDR2/LPDDR3 data mask for byte 2
B31	EBI_DM_3		P1	DO	LPDDR2/LPDDR3 data mask for byte 3
E20	EBI_DQ_0		P1	B	LPDDR2/LPDDR3 data bit 0
E22	EBI_DQ_1		P1	B	LPDDR2/LPDDR3 data bit 1
A20	EBI_DQ_2		P1	B	LPDDR2/LPDDR3 data bit 2
D21	EBI_DQ_3		P1	B	LPDDR2/LPDDR3 data bit 3
B21	EBI_DQ_4		P1	B	LPDDR2/LPDDR3 data bit 4
D23	EBI_DQ_5		P1	B	LPDDR2/LPDDR3 data bit 5
B23	EBI_DQ_6		P1	B	LPDDR2/LPDDR3 data bit 6
A24	EBI_DQ_7		P1	B	LPDDR2/LPDDR3 data bit 7
E28	EBI_DQ_8		P1	B	LPDDR2/LPDDR3 data bit 8
C26	EBI_DQ_9		P1	B	LPDDR2/LPDDR3 data bit 9

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
A26	EBI_DQ_10		P1	B	LPDDR2/LPDDR3 data bit 10
B29	EBI_DQ_11		P1	B	LPDDR2/LPDDR3 data bit 11
D29	EBI_DQ_12		P1	B	LPDDR2/LPDDR3 data bit 12
C28	EBI_DQ_13		P1	B	LPDDR2/LPDDR3 data bit 13
A30	EBI_DQ_14		P1	B	LPDDR2/LPDDR3 data bit 14
E30	EBI_DQ_15		P1	B	LPDDR2/LPDDR3 data bit 15
B17	EBI_DQ_16		P1	B	LPDDR2/LPDDR3 data bit 16
B15	EBI_DQ_17		P1	B	LPDDR2/LPDDR3 data bit 17
A14	EBI_DQ_18		P1	B	LPDDR2/LPDDR3 data bit 18
A18	EBI_DQ_19		P1	B	LPDDR2/LPDDR3 data bit 19
D15	EBI_DQ_20		P1	B	LPDDR2/LPDDR3 data bit 20
C14	EBI_DQ_21		P1	B	LPDDR2/LPDDR3 data bit 21
D17	EBI_DQ_22		P1	B	LPDDR2/LPDDR3 data bit 22
E16	EBI_DQ_23		P1	B	LPDDR2/LPDDR3 data bit 23
C34	EBI_DQ_24		P1	B	LPDDR2/LPDDR3 data bit 24
F33	EBI_DQ_25		P1	B	LPDDR2/LPDDR3 data bit 25
C36	EBI_DQ_26		P1	B	LPDDR2/LPDDR3 data bit 26
D35	EBI_DQ_27		P1	B	LPDDR2/LPDDR3 data bit 27
E34	EBI_DQ_28		P1	B	LPDDR2/LPDDR3 data bit 28
B35	EBI_DQ_29		P1	B	LPDDR2/LPDDR3 data bit 29
A34	EBI_DQ_30		P1	B	LPDDR2/LPDDR3 data bit 30
B33	EBI_DQ_31		P1	B	LPDDR2/LPDDR3 data bit 31
C24	EBI_DQS_0		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 0 (+)
E26	EBI_DQS_1		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 1 (+)
E18	EBI_DQS_2		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 2 (+)
E32	EBI_DQS_3		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 3 (+)
B25	EBI_DQS_0B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 0 (-)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
D25	EBI_DQS_1B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 1 (-)
D19	EBI_DQS_2B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 2 (-)
D31	EBI_DQS_3B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 3 (-)
J12	EBI_VREF_CA		-	AI	LPDDR2/LPDDR3 CA reference voltage
H21	EBI_VREF_D0_D2		-	AI	LPDDR2/LPDDR3 D0 and D2 reference voltage
J26	EBI_VREF_D1_D3		-	AI	LPDDR2/LPDDR3 D1 and D3 reference voltage

Table 2-5 Pin descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Primary camera serial interface – 4-lane MIPI_CSI0					
U4	MIPI_CSI0_LN0_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 0 – negative
U6	MIPI_CSI0_LN0_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 0 – positive
W6	MIPI_CSI0_CLK_N		MIPI	AI	MIPI camera serial interface 0 clock – negative
V5	MIPI_CSI0_CLK_P		MIPI	AI	MIPI camera serial interface 0 clock – positive
U2	MIPI_CSI0_LN1_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 1 – negative
T1	MIPI_CSI0_LN1_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 1 – positive
W2	MIPI_CSI0_LN2_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 2 – negative
V1	MIPI_CSI0_LN2_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 2 – positive
AA6	MIPI_CSI0_LN3_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 3 – negative
Y5	MIPI_CSI0_LN3_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 3 – positive
Secondary camera serial interface – 2-lane MIPI_CSI1					
AA2	MIPI_CSI1_LN0_N		MIPI	AI, AO	MIPI camera serial interface 1 lane 0 – negative
Y1	MIPI_CSI1_LN0_P		MIPI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AB5	MIPI_CSI1_CLK_N		MIPI	AI	MIPI camera serial interface 1 clock – negative
AB3	MIPI_CSI1_CLK_P		MIPI	AI	MIPI camera serial interface 1 clock – positive

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
AC2	MIPI_CSI1_LN1_N		MIPI	AI, AO	MIPI camera serial interface 1 lane 1 – negative
AB1	MIPI_CSI1_LN1_P		MIPI	AI, AO	MIPI camera serial interface 1 lane 1 – positive
H3	CAM_MCLK0	GPIO_26	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
C2	CAM_MCLK1	GPIO_27	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
B3	CAM_I2C_SDA	GPIO_29	P3	B B-PD:nppukp	Camera I^2C serial data Configurable I/O
F3	CAM_I2C_SCL	GPIO_30	P3	B B-PD:nppukp	Camera I^2C serial clock Configurable I/O
D3	CCI_TIMER0	GPIO_31	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O
D1	CCI_TIMER1	GPIO_32	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
B37	CCI_TIMER2	GPIO_38	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
G4	CCI_ASYNC0	GPIO_33	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/O
F1	CAM1_RST_N	GPIO_28	P3	DO B-PD:nppukp	Camera 1 (front camera) reset Configurable I/O
F5	CAM0_STANDBY_N	GPIO_34	P3	DO B-PD:nppukp	Camera 0 (rear camera) standby Configurable I/O
A4	CAM0_RSTN_N	GPIO_35	P3	DO B-PD:nppukp	Camera 0 (rear camera) reset Configurable I/O
Display serial interface – 4-lane MIPI_DSI0					
AH1	MIPI_DSI0_CLK_N		MIPI	AO	MIPI display serial interface 0 clock – negative
AG2	MIPI_DSI0_CLK_P		MIPI	AO	MIPI display serial interface 0 clock – positive
AF1	MIPI_DSI0_LN0_N		MIPI	AI, AO	MIPI display serial interface 0 lane 0 – negative
AE2	MIPI_DSI0_LN0_P		MIPI	AI, AO	MIPI display serial interface 0 lane 0 – positive
AF3	MIPI_DSI0_LN1_N		MIPI	AI, AO	MIPI display serial interface 0 lane 1 – negative
AE4	MIPI_DSI0_LN1_P		MIPI	AI, AO	MIPI display serial interface 0 lane 1 – positive
AH3	MIPI_DSI0_LN2_N		MIPI	AI, AO	MIPI display serial interface 0 lane 2 – negative

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
AG4	MIPI_DSI0_LN2_P		MIPI	AI, AO	MIPI display serial interface 0 lane 2 – positive
AL2	MIPI_DSI0_LN3_N		MIPI	AI, AO	MIPI display serial interface 0 lane 3 – negative
AK1	MIPI_DSI0_LN3_P		MIPI	AI, AO	MIPI display serial interface 0 lane 3 – positive
AB7	MIPI_DSI_LDO		MIPI	AI, AO	MIPI display serial interface 0 low-dropout regulator
AT5	MDP_VSYNC_P	GPIO_24	P3	DO B-PD:nppukp	MDP VSYNC Signal Configurable I/O
AG6	MIPI_DSI0_CAL		MIPI	AI, AO	MIPI display serial interface 0 calibration

Table 2-6 Pin descriptions – connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
High-speed USB 2.0					
AC40	USB_HS_DM			AI, AO	USB HS data minus
AB39	USB_HS_DP			AI, AO	USB HS data plus
AD35	USB_HS_SYSCLOCK			DI	USB HS system clock (19.2 MHz)
AC38	USB_HS_REXT			AI	USB HS external resistor
Secure digital controller 1 (SDC1) interface – supports dual-voltage eMMC NAND					
AE36	SDC1_CLK		P7	B-NP:pdpukp	Secure digital controller 1 clock
AH35	SDC1_CMD		P7	B-PD:nppukp	Secure digital controller 1 command
AD37	SDC1_DATA_0		P7	B-PD:nppukp	Secure digital controller 1 data bit 0
AE38	SDC1_DATA_1		P7	B-PD:nppukp	Secure digital controller 1 data bit 1
AG34	SDC1_DATA_2		P7	B-PD:nppukp	Secure digital controller 1 data bit 2
AH37	SDC1_DATA_3		P7	B-PD:nppukp	Secure digital controller 1 data bit 3
AG40	SDC1_DATA_4		P7	B-PD:nppukp	Secure digital controller 1 data bit 4
AG38	SDC1_DATA_5		P7	B-PD:nppukp	Secure digital controller 1 data bit 5
AF39	SDC1_DATA_6		P7	B-PD:nppukp	Secure digital controller 1 data bit 6
AF35	SDC1_DATA_7		P7	B-PD:nppukp	Secure digital controller 1 data bit 7

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD 3.0					
R4	SDC2_CLK		P2	BH-NP:pdpukp	Secure digital controller 2 clock
N6	SDC2_CMD		P2	BH-PD:nppukp	Secure digital controller 2 command
P3	SDC2_DATA_0		P2	BH-PD:nppukp	Secure digital controller 2 data bit 0
R6	SDC2_DATA_1		P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
T7	SDC2_DATA_2		P2	BH-PD:nppukp	Secure digital controller 2 data bit 2
P7	SDC2_DATA_3		P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
B37	SD_CARD_DET_N	GPIO_38	P3	DI PD:nppukp	Secure digital card detection Configurable I/O
G38	SD_WRITE_PROTECT	GPIO_121	P3	DI PD:nppukp	Secure digital card write protection Configurable I/O
Secure digital controller interfaces – common to all SDCs					
V9	VREF_PADS			AI	Reference for secure digital I/O pads
Dual-voltage UIM interfaces					
G40	UIM1_DATA	GPIO_57	P5	B PD:nppukp	UIM1 data Configurable I/O
J40	UIM1_CLK	GPIO_58	P5	DO PD:nppukp	UIM1 clock Configurable I/O
L38	UIM1_RESET	GPIO_59	P5	DO PD:nppukp	UIM1 reset Configurable I/O
Y39	UIM1_PRESENT	GPIO_60	P3	DI PD:nppukp	UIM1 removal detection Configurable I/O
L40	UIM2_DATA	GPIO_53	P6	B PD:nppukp	UIM2 data Configurable I/O
K39	UIM2_CLK	GPIO_54	P6	DO PD:nppukp	UIM2 clock Configurable I/O
H39	UIM2_RESET	GPIO_55	P6	DO PD:nppukp	UIM2 reset Configurable I/O
AA36	UIM2_PRESENT	GPIO_56	P3	DI PD:nppukp	UIM2 removal detection Configurable I/O
Y37	UIM3_DATA	GPIO_49	P4	B PD:nppukp	UIM3 data Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
AA34	UIM3_CLK	GPIO_50	P4	DO PD:nppukp	UIM3 clock Configurable I/O
Y35	UIM3_RESET	GPIO_51	P4	DO PD:nppukp	UIM3 reset Configurable I/O
AA38	UIM3_PRESENT	GPIO_52	P3	DI PD:nppukp	UIM3 removal detection Configurable I/O
AL38	UIM_BATT_ALARM	GPIO_61	P3	DI PD:nppukp	UIM battery alarm Configurable I/O
Y33	VREF_PADS			AI	Reference for UIM I/O pads
Sensors and keypad buttons					
G34	SMB_INT	GPIO_62	P3	DI B-PD:nppukp	SMB interrupt Configurable I/O
L36	MAG_INT	GPIO_69	P3	DI B-PD:nppukp	Magnometer interrupt Configurable I/O
E38	GYRO_ACCEL_INT_N	GPIO_115	P3	DI B-PD:nppukp	Gyro interrupt Configurable I/O
H33	KYPD_SNS0	GPIO_107	P3	DI B-PD:nppukp	Keypad sense bit 0 Configurable I/O
K35	KYPD_SNS1	GPIO_108	P3	DI B-PD:nppukp	Keypad sense bit 1 Configurable I/O
J34	KYPD_SNS2	GPIO_109	P3	DI B-PD:nppukp	Keypad sense bit 2 Configurable I/O
BAM-based low-speed peripheral interface 1 – see Table 2-2 ***for application-specific pin assignments***					
BA38	BLSP1_3	GPIO_0	P3	B PD:nppukp	BLSP 1 bit 3; UART or SPI Configurable I/O
BB39	BLSP1_2	GPIO_1	P3	B PD:nppukp	BLSP 1 bit 2; UART or SPI Configurable I/O
AV35	BLSP1_1	GPIO_2	P3	B PD:nppukp	BLSP 1 bit 1; UART, SPI, or I^2C Configurable I/O
AY37	BLSP1_0	GPIO_3	P3	B PD:nppukp	BLSP 1 bit 0; UART, SPI, or I^2C Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 2 – see Table 2-2 ***for application-specific pin assignments***					
AT9	BLSP2_3	GPIO_4	P3	B PD:nppukp	BLSP 2 bit 3; UART or SPI Configurable I/O
AY1	BLSP2_2	GPIO_5	P3	B PD:nppukp	BLSP 2 bit 2; UART or SPI Configurable I/O
AY3	BLSP2_1	GPIO_6	P3	B PD:nppukp	BLSP 2 bit 1; UART, SPI, or I^2C Configurable I/O
AV3	BLSP2_0	GPIO_7	P3	B PD:nppukp	BLSP 2 bit 0; UART, SPI, or I^2C Configurable I/O
BAM-based low-speed peripheral interface 3 – see Table 2-2 ***for application-specific pin assignments***					
H5	BLSP3_3	GPIO_8	P3	B PD:nppukp	BLSP 3 bit 3; SPI Configurable I/O
G2	BLSP3_2	GPIO_9	P3	B PD:nppukp	BLSP 3 bit 2; SPI Configurable I/O
H1	BLSP3_1	GPIO_10	P3	B PD:nppukp	BLSP 3 bit 1; SPI, or I^2C Configurable I/O
E2	BLSP3_0	GPIO_11	P3	B PD:nppukp	BLSP 3 bit 0; SPI, or I^2C Configurable I/O
BAM-based low-speed peripheral interface 4 – see Table 2-2 ***for application-specific pin assignments***					
AM39	BLSP4_3	GPIO_12	P3	B PD:nppukp	BLSP 4 bit 3; SPI Configurable I/O
AM35	BLSP4_2	GPIO_13	P3	B PD:nppukp	BLSP 4 bit 2; SPI Configurable I/O
AN40	BLSP4_1	GPIO_14	P3	B PD:nppukp	BLSP 4 bit 1; SPI, or I^2C Configurable I/O
AN36	BLSP4_0	GPIO_15	P3	B PD:nppukp	BLSP 4 bit 0; SPI, or I^2C Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 2-2 ***for application-specific pin assignments***					
K7	BLSP5_3	GPIO_16	P3	B PD:nppukp	BLSP 5 bit 3; SPI Configurable I/O
G6	BLSP5_2	GPIO_17	P3	B PD:nppukp	BLSP 5 bit 2; SPI Configurable I/O
J6	BLSP5_1	GPIO_18	P3	B PD:nppukp	BLSP 5 bit 1; SPI, or I^2C Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
J4	BLSP5_0	GPIO_19	P3	B PD:nppukp	BLSP 5 bit 0; SPI, or I²C Configurable I/O
BAM-based low-speed peripheral interface 6 – see Table 2-2 ***for application-specific pin assignments***					
AY7	BLSP6_3	GPIO_20	P3	B PD:nppukp	BLSP 6 bit 3; SPI Configurable I/O
AW6	BLSP6_3	GPIO_21	P3	B PD:nppukp	BLSP 6 bit 2; SPI Configurable I/O
AV7	BLSP6_3	GPIO_22	P3	B PD:nppukp	BLSP 6 bit 1; SPI, or I²C Configurable I/O
BA2	BLSP6_3	GPIO_23	P3	B PD:nppukp	BLSP 3 bit 0; SPI, or I²C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol) signals					
AT9	BLSP1_SPI_CS3_N	GPIO_4	P3	B PD:nppukp	BLSP 1 Chip select 3 Configurable I/O
AY1	BLSP2_SPI_CS3_N	GPIO_5	P3	B PD:nppukp	BLSP 2Chip select 3 Configurable I/O
K7	BLSP1_SPI_CS2_N	GPIO_16	P3	B PD:nppukp	BLSP 1 Chip select 2 Configurable I/O
G6	BLSP2_SPI_CS2_N	GPIO_17	P3	B PD:nppukp	BLSP 2 Chip select 2 Configurable I/O
E4	BLSP3_SPI_CS2_N	GPIO_37	P3	B PD:nppukp	BLSP 3 Chip select 2 Configurable I/O
L36	BLSP3_SPI_CS3_N	GPIO_69	P3	B PD:nppukp	BLSP 3 Chip select 3 Configurable I/O
B39	BLSP1_SPI_CS1_N	GPIO_110	P3	B PD:nppukp	BLSP 1 Chip select 1 Configurable I/O
F39	BLSP3_SPI_CS1_N	GPIO_120	P3	B PD:nppukp	BLSP 3 Chip select 1 Configurable I/O
G38	BLSP2_SPI_CS1_N	GPIO_121	P3	B PD:nppukp	BLSP 2 Chip select 1 Configurable I/O
Audio clock					
AW38	Audio_MCLK	GPIO_116	P3	B PD:nppukp	Audio Master CLK signal Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Audio MI2S interface #1					
D39	SPKR_SCLK	GPIO_113	P3	B PD:nppukp	Speaker SCLK signal Configurable I/O
B39	SPKR_WS	GPIO_110	P3	B PD:nppukp	Speaker Word Select signal Configurable I/O
E40	SPKR_D0	GPIO_114	P3	B PD:nppukp	Speaker Data0 signal Configurable I/O
E38	SPKR_D1	GPIO_115	P3	B PD:nppukp	Speaker Data1 signal Configurable I/O
Audio MI2S interface #2					
AR36	MI2S_SCLK	GPIO_118	P3	B PD:nppukp	MI2S SCLK signal Configurable I/O
AV37	MI2S_WS	GPIO_117	P3	B PD:nppukp	MI2S Word Select signal Configurable I/O
BA40	MI2S_D0	GPIO_119	P3	B PD:nppukp	MI2S Data0 signal Configurable I/O
AW36	MI2S_D1	GPIO_112	P3	B PD:nppukp	MI2S Data1 signal Configurable I/O
Digital MIC interface					
BA38	DMIC0_CLK	GPIO_0	P3	DO PD:nppukp	Digital MIC0 clock Configurable I/O
BB39	DMIC0_DATA	GPIO_1	P3	B PD:nppukp	Digital MIC0 data Configurable I/O

2.2.1.1 General purpose clocks, PDM, and related signals

The APQ8016 IC has several general purpose clock outputs, as well as general purpose pulse density modulated (PDM) outputs:

- GP_PDM – a configurable pulse-density output (12-bit value configurable), with the base frequency set at 4.8 MHz.
  - The APQ8016 supports three different instances of this configurable PDM output
  - GP_PDM0, 1, and 2 can each be used independently. If there is an A or B option in the IO name, it means only one or the other can be used.

- GP_CLK – A general purpose clock output that lets the user configure a desired clock output by first selecting a clock source (GPLL0 or 19.2 MHz) and then programming a desired division ratio (M/N) and a duty cycle.
  - The APQ8016 supports four different instances of this clock output
  - GP_CLK0, 1, 2, and 3 can be used independently. If there is an A or B option in the IO name, it means only one or the other can be used.
  - Different division ratios may result in differing jitter, with integer divisors producing the cleanest outputs.
- GP_MN – Similar to GP_CLK, except the source clock is always 4.8 MHz. It is only available behind GPIO110.

Table 2-7 Pin descriptions – internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
JTAG interface					
K1	SRST_N		P3	PU	JTAG reset for debug
M1	TCK		P3	PU	JTAG clock input
M3	TDI		P3	PU:nppdkp	JTAG data input
J2	TDO		P3		JTAG data output
L2	TMS		P3	PU:nppdkp	JTAG mode-select input
K3	TRST_N		P3	PD	JTAG reset
General purpose clocks, PDM and related signals					
AY7	GP_PDM_0A	GPIO_20	P3	DO B-PD:nppukp	General-purpose PDM output 0A, 12-bit, XO/4 clock Configurable I/O
AA38	GP_PDM_1A	GPIO_52	P3	DO B-PD:nppukp	General-purpose PDM output 1A, 12-bit, XO/4 clock Configurable I/O
AU4	GP_PDM_0B	GPIO_25	P3	DO B-PD:nppukp	General-purpose PDM output 0B, 12-bit, XO/4 clock Configurable I/O
AW6	GP_PDM_1B	GPIO_21	P3	DO B-PD:nppukp	General-purpose PDM output 1B, 12-bit, XO/4 clock Configurable I/O
A38	GP_PDM_2A	GPIO_98	P3	DO B-PD:nppukp	General-purpose PDM output 2A, 12-bit, XO/4 clock Configurable I/O
D39	GP_PDM_2B	GPIO_113	P3	DO B-PD:nppukp	General-purpose PDM output 2B, 12-bit, XO/4 clock Configurable I/O
D3	GP_CLK0	GPIO_31	P3	DO B-PD:nppukp	General-purpose clock 0 Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
D1	GP_CLK1	GPIO_32	P3	DO B-PD:nppukp	General-purpose clock 1 Configurable I/O
Y37	GP_CLK_1A	GPIO_49	P4	DO B-PD:nppukp	General-purpose clock 1A Configurable I/O
AA34	GP_CLK_2A	GPIO_50	P4	DO B-PD:nppukp	General-purpose clock 2A Configurable I/O
Y35	GP_CLK_3A	GPIO_51	P4	DO B-PD:nppukp	General-purpose clock 3A Configurable I/O
C38	GP_CLK_1B	GPIO_97	P3	DO B-PD:nppukp	General-purpose clock 1B Configurable I/O
AM39	GP_CLK_2B	GPIO_12	P3	DO B-PD:nppukp	General-purpose clock 2B Configurable I/O
AM35	GP_CLK_3B	GPIO_13	P3	DO B-PD:nppukp	General-purpose clock 3B Configurable I/O
B39	GP_MN	GPIO_110	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
Resets and mode controls					
AU32 AT31	MODE_0 and MODE_1		P3	DIS-PD	Mode_0 and Mode_1 pins control the operating mode of the device, per the following truth table: “00” | Native Mode, used for normal operation “11” | Test mode, can be used for JTAG Boundary Scan testing All other modes are reserved.
AV1	RESOUT_N		P3	DO	Reset output
E4	FORCED_USB_BOOT	GPIO[37]	P3	DI B-PD:nppukp	Force USB boot control Configurable I/O
C38	BOOT_CONFIG[14]	GPIO[97]	P3	DI B-PD:nppukp	Boot Configuration pins [14:0] control various secure boot, debugging, and boot device options. Many of these options are hard-wired on shipped devices via qFUSE settings. As immediate reference, the most often used pins during board development stage are BOOT_CONFIG[3:1], which directly control the boot device used, per the following truth table: “000” | SDC1, followed by SDC2 if needed. “001” | SDC2, followed by SDC1 if needed. “010” | SDC1 only “011” | USB
BC34	BOOT_CONFIG[13]	GPIO[94]	P3	DI B-PD:nppukp	
BD33	BOOT_CONFIG[12]	GPIO[93]	P3	DI B-PD:nppukp	
AY33	BOOT_CONFIG[11]	GPIO[92]	P3	DI B-PD:nppukp	
BE38	BOOT_CONFIG[10]	GPIO[91]	P3	DI B-PD:nppukp	

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
BA32	BOOT_CONFIG[9]	GPIO[90]	P3	DI B-PD:nppukp	
BD35	BOOT_CONFIG[8]	GPIO[89]	P3	DI B-PD:nppukp	
BB35	BOOT_CONFIG[7]	GPIO[88]	P3	DI B-PD:nppukp	
BB37	BOOT_CONFIG[6]	GPIO[87]	P3	DI B-PD:nppukp	
BD39	BOOT_CONFIG[5]	GPIO[86]	P3	DI B-PD:nppukp	
BC8	BOOT_CONFIG[4]	GPIO[84]	P3	DI B-PD:nppukp	
BC40	BOOT_CONFIG[3]	GPIO[83]	P3	DI B-PD:nppukp	
BC38	BOOT_CONFIG[2]	GPIO[82]	P3	DI B-PD:nppukp	
BD7	BOOT_CONFIG[1]	GPIO[81]	P3	DI B-PD:nppukp	
BD5	BOOT_CONFIG[0]	GPIO[80]	P3	DI B-PD:nppukp	

Table 2-8 APQ8016 wakeup pins for modem power management (MPM)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
BB39	GPIO_1	P3	B-PD:nppukp	General purpose wakeup
AY1	GPIO_5	P3	B-PD:nppukp	General purpose wakeup
G2	GPIO_9	P3	B-PD:nppukp	General purpose wakeup
E2	GPIO_11	P3	B-PD:nppukp	General-purpose wakeup
AM39	GPIO_12	P3	B-PD:nppukp	General-purpose wakeup
AM35	GPIO_13	P3	B-PD:nppukp	General-purpose wakeup
AY7	GPIO_20	P3	B-PD:nppukp	General-purpose wakeup
AW6	GPIO_21	P3	B-PD:nppukp	General-purpose wakeup

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
AU4	GPIO_25	P3	B-PD:nppukp	General-purpose wakeup
F1	GPIO_28	P3	B-PD:nppukp	General-purpose wakeup
D3	GPIO_31	P3	B-PD:nppukp	General-purpose wakeup
F5	GPIO_34	P3	B-PD:nppukp	General-purpose wakeup
A4	GPIO_35	P3	B-PD:nppukp	General-purpose wakeup
C4	GPIO_36	P3	B-PD:nppukp	General-purpose wakeup
E4	GPIO_37	P3	B-PD:nppukp	General-purpose wakeup
B37	GPIO_38	P3	B-PD:nppukp	General-purpose wakeup
Y37	GPIO_49	P4	B-PD:nppukp	General-purpose wakeup
AA34	GPIO_50	P4	B-PD:nppukp	General-purpose wakeup
Y35	GPIO_51	P4	B-PD:nppukp	General-purpose wakeup
AA38	GPIO_52	P3	B-PD:nppukp	General-purpose wakeup
K39	GPIO_54	P3	B-PD:nppukp	General-purpose wakeup
G34	GPIO_62	P3	B-PD:nppukp	General-purpose wakeup
AJ38	GPIO_66	P3	B-PD:nppukp	General-purpose wakeup
AL40	GPIO_68	P3	B-PD:nppukp	General-purpose wakeup
L36	GPIO_69	P3	B-PD:nppukp	General-purpose wakeup
C38	GPIO_97	P3	B-PD:nppukp	General-purpose wakeup
A38	GPIO_98	P3	B-PD:nppukp	General-purpose wakeup
H33	GPIO_107	P3	B-PD:nppukp	General-purpose wakeup
K35	GPIO_108	P3	B-PD:nppukp	General-purpose wakeup
J34	GPIO_109	P3	B-PD:nppukp	General-purpose wakeup
B39	GPIO_110	P3	B-PD:nppukp	General-purpose wakeup
C40	GPIO_111	P3	B-PU:nppukp	General-purpose wakeup
AW36	GPIO_112	P3	B-PD:nppukp	General-purpose wakeup
D39	GPIO_113	P3	B-PD:nppukp	General-purpose wakeup
E40	GPIO_114	P3	B-PD:nppukp	General-purpose wakeup

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
E38	GPIO_115	P3	B-PD:nppukp	General-purpose wakeup
AV37	GPIO_117	P3	B-PD:nppukp	General-purpose wakeup
AR36	GPIO_118	P3	B-PD:nppukp	General-purpose wakeup
F39	GPIO_120	P3	B-PD:nppukp	General-purpose wakeup
G38	GPIO_121	P3	B-PD:nppukp	General-purpose wakeup
AE38	SDC1_DATA_1	P7	B-PD:nppukp	SDIO wakeup
AH37	SDC1_DATA_3	P7	B-PD:nppukp	SD card detect
R6	SDC2_DATA_1	P2	BH-PD:nppukp	SDIO wakeup
P7	SDC2_DATA_3	P2	BH-PD:nppukp	SD card detect
K1	SRST_N	P3	DI	JTAG

[1] Refer to Table 2-3 for parameter and acronym definitions.

Table 2-9 Pin descriptions – chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
RFIC – GNSS Rx baseband interface					
BE12	GNSS_BB_IP		-	AI	GNSS receiver baseband input, in-phase plus
BD11	GNSS_BB_IM		-	AI	GNSS receiver baseband input, in-phase minus
BC14	GNSS_BB_QP		-	AI	GNSS receiver baseband input, quadrature plus
BB13	GNSS_BB_QM		-	AI	GNSS receiver baseband input, quadrature minus
RFIC – status and control signals					
AT35	SSBI_WTR0_RX	GPIO_103	P3	B B-PD:nppukp	SSBI 1 for RFIC 0 Configurable I/O
AW40	SSBI_WTR0_TX	GPIO_104	P3	B B-PD:nppukp	SSBI 2 for RFIC 0 Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
AU36	SSBI_WTR1_RX	GPIO_105	P3	B B-PD:nppukp	SSBI 1 for RFIC 1 Configurable I/O
AY39	SSBI_WTR1_TX	GPIO_106	P3	B B-PD:nppukp	SSBI 2 for RFIC 1 Configurable I/O
WCN – WLAN signals					
BD3	WLAN_DATA0	GPIO_42	P3	B B-PD:nppukp	WLAN data bit 0 Configurable I/O
BB1	WLAN_DATA1	GPIO_41	P3	B B-PD:nppukp	WLAN data bit 1 Configurable I/O
BB5	WLAN_DATA2	GPIO_40	P3	B B-PD:nppukp	WLAN data bit 2 Configurable I/O
BB3	WLAN_CLK	GPIO_44	P3	DO-Z B-PD:nppukp	WLAN Clock Configurable I/O
BA6	WLAN_SET	GPIO_43	P3	DO-Z B-PD:nppukp	WLAN Set Configurable I/O
AR14	WLAN_BB_IM		-	AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
AP15	WLAN_BB_IP		-	AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
AP13	WLAN_BB_QM		-	AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
AR12	WLAN_BB_QP		-	AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
AU14	WLAN_REXT		-	AI	WLAN external resistor
AR8	WLAN_XO		-	DI	WLAN clock
WCN – Bluetooth signals					
AW8	BT_DATA	GPIO_48	P3	B B-PD:nppukp	Bluetooth dual-function signal – serial data and strobe Configurable I/O
BA4	BT_CTL	GPIO_47	P3	DO B-PD:nppukp	Bluetooth control Configurable I/O
BC2	BT_SSBI	GPIO_39	P3	B B-PD:nppukp	Bluetooth single-wire serial bus interface Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
WCN – FM signals					
AY9	FM_DATA	GPIO_46	P3	B B-PD:nppukp	FM radio serial data interface Configurable I/O
AY5	FM_SSBI	GPIO_45	P3	B B-PD:nppukp	FM radio single-wire serial bus interface Configurable I/O
PMIC interfaces					
AK37	PMIC_SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – data
AJ36	PMIC_SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – clock
E36	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
F35	RESIN_N		P3	DI	Reset input
G36	SLEEP_CLK		P3	DI	Sleep clock
AL34	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz
A36	CXO_EN		P3	DO	Core crystal oscillator enable
GPS control					
BC32	EXT_GPS_LNA_EN	GPIO_96	P3	DO PD:nppukp	EXT_GPS_LNA_EN Configurable I/O

Table 2-10 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
BA38	GPIO_0	 BLSP1_3 DMIC0_CLK	P3	B-PD:nppukp B DO	Configurable I/O BLSP #1, bit 3; UART or SPI Digital MIC0 clock
BB39	GPIO_1	 BLSP1_2 DMIC0_DATA	P3	B-PD:nppukp B DI	Configurable I/O BLSP #1, bit 2; UART or SPI Digital MIC0 data
AV35	GPIO_2	 BLSP1_1	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 1; UART, SPI or I^2C
AY37	GPIO_3	 BLSP1_0	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 0; UART, SPI or I^2C

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
AT9	GPIO_4	BLSP2_3 BLSP1_SPI_CS3_N	P3	B-PD:nppukp B DO	Configurable I/O BLSP #2, bit 3; UART or SPI Chip select 3 for SPI on BLSP1
AY1	GPIO_5	BLSP2_2 BLSP2_SPI_CS3_N	P3	B-PD:nppukp B DO	Configurable I/O BLSP #2, bit 2; UART or SPI Chip select 3 for SPI on BLSP2
AY3	GPIO_6	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; UART, SPI, or I^2C
AV3	GPIO_7	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; UART, SPI, or I^2C
H5	GPIO_8	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; SPI or I^2C
G2	GPIO_9	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI or I^2C
H1	GPIO_10	BLSP3_1	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 1; SPI, or I^2C
E2	GPIO_11	BLSP3_0	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 0; SPI, or I^2C
AM39	GPIO_12	BLSP4_3 GP_CLK_2B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #4, bit 3; SPI, or I^2C General-purpose clock output 2B
AM35	GPIO_13	BLSP4_2 GP_CLK_3B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #4, bit 2; SPI, or I^2C General-purpose clock output 3B
AN40	GPIO_14	BLSP4_1	P3	B-PD:nppukp B	Configurable I/O BLSP #4, bit 1; SPI, or I^2C
AN36	GPIO_15	BLSP4_0	P3	B-PD:nppukp B	Configurable I/O BLSP #4, bit 0; SPI, or I^2C
K7	GPIO_16	BLSP5_3 BLSP1_SPI_CS2_N	P3	B-PD:nppukp B DO	Configurable I/O BLSP #5, bit 3; SPI, or I^2C Chip select 2 for SPI on BLSP1
G6	GPIO_17	BLSP5_2 BLSP2_SPI_CS2_N	P3	B-PD:nppukp B DO	Configurable I/O BLSP #5, bit 2; SPI, or I^2C Chip select 2 for SPI on BLSP1
J6	GPIO_18	BLSP5_1	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 1; SPI, or I^2C
J4	GPIO_19	BLSP5_0	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 0; SPI, or I^2C

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
AY7	GPIO_20	BLSP6_3 GP_PDM_0A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #6, bit 3; SPI, or I^2C General-purpose PDM output 0A, 12-bit, XO/4 clock
AW6	GPIO_21	BLSP6_2 GP_PDM_1B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #6, bit 2; SPI, or I^2C General-purpose PDM output 1B, 12-bit, XO/4 clock
AV7	GPIO_22	BLSP6_1	P3	B-PD:nppukp B	Configurable I/O BLSP #6, bit 1; SPI, or I^2C
BA2	GPIO_23	BLSP6_0	P3	B-PD:nppukp B	Configurable I/O BLSP #6, bit 0; SPI, or I^2C
AT5	GPIO_24	MDP_VSYNC_P	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – primary
AU4	GPIO_25	DSI_RST_N GP_PDM_0B	P3	B-PD:nppukp DO DO	Configurable I/O Display reset General-purpose PDM output 0B, 12-bit, XO/4 clock
H3	GPIO_26	CAM_MCLK0	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 0
C2	GPIO_27	CAM_MCLK1	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 1
F1	GPIO_28	CAM1_RST_N	P3	B-PD:nppukp DO	Configurable I/O Camera 1 (front camera) reset
B3	GPIO_29	CAM_I2C_SDA	P3	B-PD:nppukp B	Configurable I/O Camera control interface I^2C 0 serial data
F3	GPIO_30	CAM_I2C_SCL	P3	B-PD:nppukp B	Configurable I/O Camera control interface I^2C 0 serial Clock
D3	GPIO_31	CCI_TIMER0 GP_CLK0	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 0 General-purpose clock 0
D1	GPIO_32	CCI_TIMER1 GP_CLK1	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 1 General-purpose clock 1
G4	GPIO_33	CCI_ASYNC0	P3	B-PD:nppukp DI	Configurable I/O Camera control interface async 0
F5	GPIO_34	CAM0_STANDBY_N	P3	B-PD:nppukp DO	Configurable I/O Camera 0 (rear camera) standby

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
A4	GPIO_35	CAM0_RST_N	P3	B-PD:nppukp DO	Configurable I/O Camera 0 (rear camera) reset
C4	GPIO_36	FLASH_LED_RESET	P3	B-PD:nppukp DO	Configurable I/O LED Flash reset
E4	GPIO_37	BLSP3_SPI_CS2_N FORCED_USB_BOOT	P3	B-PD:nppukp DO DI	Configurable I/O Chip select 2 for SPI on BLSP3 Force USB boot control
B37	GPIO_38	SD_CARD_DET_N CCI_TIMER2	P3	B-PD:nppukp DI DO	Configurable I/O Secure digital card detection Camera control interface timer 2
BC2	GPIO_39	BT_SSBI	P3	B-PD:nppukp B	Configurable I/O Bluetooth single-wire serial bus interface
BB5	GPIO_40	WLAN_DATA2	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 2
BB1	GPIO_41	WLAN_DATA1	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 1
BD3	GPIO_42	WLAN_DATA0	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 0
BA6	GPIO_43	WLAN_SET	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN set
BB3	GPIO_44	WLAN_CLK	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN clock
AY5	GPIO_45	FM_SSBI	P3	B-PD:nppukp B	Configurable I/O FM-radio SSBI
AY9	GPIO_46	FM_DATA	P3	B-PD:nppukp B	Configurable I/O FM radio serial data interface
BA4	GPIO_47	BT_CTL	P3	B-PD:nppukp DO	Configurable I/O Bluetooth control
AW8	GPIO_48	BT_DATA	P3	B-PD:nppukp B	Configurable I/O Bluetooth dual function: data and strobe
Y37	GPIO_49	UIM3_DATA GP_CLK_1A	P4	B-PD:nppukp B DO	Configurable I/O UIM3 data General-purpose clock output 1A
AA34	GPIO_50	UIM3_CLK GP_CLK_2A	P4	B-PD:nppukp DO DO	Configurable I/O UIM3 clock General-purpose clock output 2A

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
Y35	GPIO_51	UIM3_RST GP_CLK_3A	P4	B-PD:nppukp DO DO	Configurable I/O UIM3 reset General-purpose clock output 3A
AA38	GPIO_52	UIM3_PRESENT GP_PDM_1A	P3	B-PD:nppukp DI DO	Configurable I/O UIM3 removal detection General-purpose PDM output 1A, 12-bit, XO/4 clock
L40	GPIO_53	UIM2_DATA	P6	B-PD:nppukp B	Configurable I/O UIM2 data
K39	GPIO_54	UIM2_CLK	P6	B-PD:nppukp DO	Configurable I/O UIM2 clock
H39	GPIO_55	UIM2_RST	P6	B-PD:nppukp DO	Configurable I/O UIM2 reset
AA36	GPIO_56	UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 removal detection
G40	GPIO_57	UIM1_DATA	P5	B-PD:nppukp B	Configurable I/O UIM1 data
J40	GPIO_58	UIM1_CLK	P5	B-PD:nppukp DO	Configurable I/O UIM1 clock
L38	GPIO_59	UIM1_RST	P5	B-PD:nppukp DO	Configurable I/O UIM1 reset
Y39	GPIO_60	UIM1_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM1 removal detection
AL38	GPIO_61	UIM_BATT_ALARM	P3	B-PD:nppukp DI	Configurable I/O UIM battery alarm
G34	GPIO_62	SMB_INT	P3	B-PD:nppukp DI	Configurable I/O SMB interrupt
AJ40	GPIO_63	CDC_PDM0_CLK[1]	P3	B-PD:nppukp DO	Configurable I/O PDM0 Clock
AH39	GPIO_64	CDC_PDM0_SYNC[1]	P3	B-PD:nppukp DO	Configurable I/O PDM0 sync signal
AK39	GPIO_65	CDC_PDM0_TX0[1]	P3	B-PD:nppukp DI	Configurable I/O PDM0 Transmit signal 0
AJ38	GPIO_66	CDC_PDM0_RX0[1]	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 0
AK35	GPIO_67	CDC_PDM0_RX1[1]	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 1

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
AL40	GPIO_68	CDC_PDM0_RX2[1]	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 2
L36	GPIO_69	MAG_INT BLSP3_SPI_CS3_N	P3	B-PD:nppukp DI DO	Configurable I/O Magnometer interrupt Chip select 3 for SPI on BLSP3
AN38	GPIO_70		P3	B-PD:nppukp	Configurable I/O
AR38	GPIO_71		P3	B-PD:nppukp	Configurable I/O
AT39	GPIO_72		P3	B-PD:nppukp	Configurable I/O
AU40	GPIO_73		P3	B-PD:nppukp	Configurable I/O
AP37	GPIO_74		P3	B-PD:nppukp	Configurable I/O
AV39	GPIO_75		P3	B-PD:nppukp	Configurable I/O
AP35	GPIO_76		P3	B-PD:nppukp	Configurable I/O
BC4	GPIO_77		P3	B-PD:nppukp	Configurable I/O
BE4	GPIO_78		P3	B-PD:nppukp	Configurable I/O
BC6	GPIO_79		P3	B-PD:nppukp	Configurable I/O
BD5	GPIO_80	BOOT_CONFIG_0 (WDOG_DISABLE)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 0
BD7	GPIO_81	BOOT_CONFIG_1	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 1
BC38	GPIO_82	BOOT_CONFIG_2	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 2
BC40	GPIO_83	BOOT_CONFIG_3	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 3
BC8	GPIO_84	BOOT_CONFIG_4	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 4
BE6	GPIO_85	SDC1_EMMC_1P2_EN	P3	B-PD:nppukp DI	Configurable I/O Enables 1.2 V I/O for eMMC on SDC1
BD39	GPIO_86	BOOT_CONFIG_5	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 5
BB37	GPIO_87	BOOT_CONFIG_6	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 6

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
BB35	GPIO_88	BOOT_CONFIG_7	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 7
BD35	GPIO_89	BOOT_CONFIG_8	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 8
BA32	GPIO_90	BOOT_CONFIG_9	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 9
BE38	GPIO_91	BOOT_CONFIG_10	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 10
AY33	GPIO_92	BOOT_CONFIG_11	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 11
BD33	GPIO_93	BOOT_CONFIG_12	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 12
BC34	GPIO_94	BOOT_CONFIG_13	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 13
BB31	GPIO_95		P3	B-PD:nppukp	Configurable I/O
BC32	GPIO_96	EXT_GNSS_LNA_EN	P3	B-PD:nppukp DO	Configurable I/O External GNSS LNA enable
C38	GPIO_97	LCD_DRIVER_5V_EN GP_CLK_1B BOOT_CONFIG_14	P3	B-PD:nppukp DO DO DI	Configurable I/O 5 V display driver enable General-purpose clock output 1B Boot configuration control bit 14
A38	GPIO_98	LCD_BL_EN GP_PDM_2A	P3	B-PD:nppukp DO DO	Configurable I/O Display backlight enable General-purpose PDM 2A output
BE34	GPIO_99		P3	B-PD:nppukp	Configurable I/O
BE36	GPIO_100		P3	B-PD:nppukp	Configurable I/O
BB33	GPIO_101		P3	B-PD:nppukp	Configurable I/O
BE32	GPIO_102		P3	B-PD:nppukp	Configurable I/O
AT35	GPIO_103	SSBI_WTR0_RX	P3	B-PD:nppukp B	Configurable I/O SSBI 1 for RFIC 0
AW40	GPIO_104	SSBI_WTR0_TX	P3	B-PD:nppukp B	Configurable I/O SSBI 2 for RFIC 0
AU36	GPIO_105	SSBI_WTR1_RX	P3	B-PD:nppukp B	Configurable I/O SSBI 1 for RFIC 1
AY39	GPIO_106	SSBI_WTR1_TX	P3	B-PD:nppukp B	Configurable I/O SSBI 2 for RFIC 1

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
H33	GPIO_107	KYPD_SNS0	P3	B-PD:nppukp DI	Configurable I/O Keypad sense bit 0
K35	GPIO_108	KYPD_SNS1	P3	B-PD:nppukp DI	Configurable I/O Keypad sense bit 1
J34	GPIO_109	KYPD_SNS2	P3	B-PD:nppukp DI	Configurable I/O Keypad sense bit 2
B39	GPIO_110	BLSP1_SPI_CS1_N MI2S_1_WS GP_MN USB_HS_ID	P3	B-PD:nppukp DO B DO DI	Configurable I/O Chip select 1 for SPI on BLSP1 MI2S #1 word select (L/R) General-purpose M/N:D counter output USB ID pin for host mode detection
C40	GPIO_111		P3	B-PU:nppukp	Configurable I/O
AW36	GPIO_112	MI2S_2_D1	P3	B-PD:nppukp B	Configurable I/O MI2S #2 serial data channel 1
D39	GPIO_113	MI2S_1_SCLK GP_PDM_2B	P3	B-PD:nppukp B DO	Configurable I/O MI2S #1 bit clock General-purpose PDM 2B output
E40	GPIO_114	MI2S_1_D0	P3	B-PD:nppukp B	Configurable I/O MI2S #1 serial data channel 0
E38	GPIO_115	GYRO_ACCEL_INT_N MI2S_1_D1	P3	B-PD:nppukp DI B	Configurable I/O Gyro interrupt MI2S #1 serial data channel 1
AW38	GPIO_116	MI2S_1_MCLK	P3	B-PD:nppukp DO	Configurable I/O MI2S #1 master clock
AV37	GPIO_117	MI2S_2_WS	P3	B-PD:nppukp B	Configurable I/O MI2S #2 word select (L/R)
AR36	GPIO_118	MI2S_2_SCLK	P3	B-PD:nppukp B	Configurable I/O MI2S #2 bit clock
BA40	GPIO_119	MI2S_2_D0	P3	B-PD:nppukp B	Configurable I/O MI2S #2 serial data channel 0
F39	GPIO_120	BLSP3_SPI_CS1_N	P3	B-PD:nppukp DO	Configurable I/O Chip select 1 for SPI on BLSP3
G38	GPIO_121	BLSP2_SPI_CS1_N	P3	B-PD:nppukp DO	Configurable I/O Chip select 2 for SPI on BLSP2

[1] This is a PDM interface specific to the QC Codec used in this chipset, as opposed to the general purpose PDM available on another set of IOs.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-10 for a list of all supported functions for each GPIO.

NOTE: System designers must examine each GPIO's external connection and programmed configuration, and take necessary steps to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, an Excel spreadsheet is provided that lists all APQ8016 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

You can download this spreadsheet *APQ8016 GPIO Pin Assignments* (LM80-P0436-6) at: https://www.qualcomm.com/products/snapdragon/embedded-computing.

Table 2-11 Pin descriptions – No connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
A2, A40, AB11, AB19, AB23, AC6, AD1, AD23, AD27, AD3, AD31, AD5, AJ6, AK25, AK27, AK3, AK5, AL4, AL6, AM27, AM5, AM7, AN2, AN4, AN6, AP25, AP3, AP5, AP7, AT1, AT17, AT19, AT21, AT25, AT3, AU16, AU18, AU2, AU20, AU24, AV21, AV23, AV25, AV27, AV29, AV31, AW16, AW18, AW20,AW22, AW24, AW26, AW28, AW30, AW32, AY19, AY25, AY29, B1, BA18, BA20, BA24, BA30, BB15, BB17, BB21, BB29, BB9, BC16, BC20, BC30, BD1, BD15, BD21, BD29, BD9, BE14, BE2, BE20, BE40, D33, D37, F15, F17, F21, G22, G26, H11, H13, H15, H19, H23, H25, H27, H29, H31, H7, M19, P19, P23, P25, AA40	NC	No connect; not connected internally
BA36, AY35, AN8, AY15, AY17, BA14, BA16	DNC	Do not connect; connected internally, do not connect externally

Table 2-12 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
AP17	VDD_A1	Power for analog circuits – low voltage
AP19	GND	GND for APQ

Pad #	Pad name	Functional description
AR18, AR20	VDD_A2	Power for analog circuits – high voltage
AR22, AR24	GND	GND for APQ
AB25, AB27, AB29, AB31, K29, K31, K33, M23, M25, M27, M29, M31, M33, P27, P29, P31, P33, T25, T27, T29, T33, V25, V27, V29, V31, V33, Y25, Y27, Y29, Y31	VDD_APC	Power for applications microprocessors
AF31, U8, AD13, AD15, AD17, AD25, AD29, AH11, AH17, AH19, AH21, AM17, AM19, AR10, M11, M21, M9, T11, T21, T9, U22, U24, Y11, Y13, Y15, Y17, Y9	VDD_CORE	Power for digital core circuits
AD11, AG28, AH13, AH15, AH23, AH25, AH27, AH29, AJ28, AL28, AM11, AM9, AN28, AP29, AU10, K25, M15, N14, T13, T15, T23, T31, Y19, J28, K27, M13, M17, AP27	VDD_MEM	Power for on-chip memory
AE6, AE8, AB9, AC8	VDD_MIPI	Power for MIPI circuits (CSI and DSI)
AH5	VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL
J10, J14, J20, J22, J24, J30, K11, K15, K19, K23	VDD_P1	Power for pad group 1 – EBI pads
W8	VDD_P2	Power for pad group 2 – SDC2 pads
AA32, AG32, AK9, AP33, AT11, AT33, AT7, AU30, AU34, AU8, F31, H17, J8, V7	VDD_P3	Power for pad group 3 – most I/O pads
AB35	VDD_P4	Power for pad group 4 – UIM3 pads
L34	VDD_P5	Power for pad group 5 – UIM1 pads
AC34	VDD_P6	Power for pad group 6 – UIM2 pads
AF33	VDD_P7	Power for pad group 7 – SDC1 pads
Y21, AG16, AE22	VDD_PLL1	Power for PLL circuits – low voltage
W24, AP23, AN14	VDD_PLL2	Power for PLL circuits – high voltage
AJ8	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise GND
AE30	VDD_USB_HS	Power for USB PHY interface – digital voltage
AD33	VDD_USBPHY_1P8	Power for USB PHY interface – low voltage
AC32	VDD_USBPHY_3P3	Power for USB PHY interface – high voltage
AT15	VDD_WLAN	Power for WLAN ADC circuits

Table 2-13 Pin descriptions – ground pins

Pad #	Pad name	Functional description
A12, A16, A22, A28, A32, A6, AA24, AA26, AA28, AA30, AA4, AA8, AB13, AB15, AB17, AB21, AC30, AC4, AD19, AD21, AD7, AE16, AE20, AF11, AF13, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AF29, AF5, AF9, AG18, AG20, AH31, AH7, AH9, AJ2, AJ34, AJ4, AK11, AK13, AK15, AK17, AK19, AK21, AK23, AK29, AK31, AK33, AK7, AL30, AL8, AM1, AM13, AM15, AM21, AM23, AM25, AM29, AM3, AM31, AM33, AN20, AP9, AR26, AR4, AR6, AT13, AT23, AT27, AT29, AU12, AU22, AU26, AU28, AU38, AU6, AV11, AV13, AV15, AV17, AV19, AV33, AV5, AV9, AW10, AW12, AW14, AW2, AW34, AW4, AY11, AY13, AY21, AY23, AY27, B5, BA12, BA22, BA26, BA28, BA8, BB19, BB23, BB25, BB27, BB7, BC12, BC18, BC22, BC24, BC26, BC28, BC36, BD13, BD17, BD19, BD23, BD25, BD27, BD37, BE10, BE16, BE18, BE22, BE24, BE26, BE28, BE8, C18, C20, C32, C8, D27, D5, D7, E12, F19, F25, F27, F29, F37, F7, G10, G12, G14, G16, G18, G20, G24, G28, G30, G32, G8, H35, H37, J16, J18, J32, J36, J38, K17, K21, K37, K5, K9, L30, L32, L4, L6, L8, M35, M37, M39, M5, M7, N2, N22, N24, N26, N28, N30, N32, N34, N36, N38, N4, N40, N8, P11, P13, P15, P17, P21, P35, P37, P39, P5, P9, R22, R24, R26, R28, R30, R32, R34, R36, R38, R40, R8, T17, T19, T3, T35, T37, T39, T5, U26, U28, U30, U32, U34, U36, U38, U40, V11, V13, V15, V17, V19, V21, V23, V3, V35, V37, V39, W16, W22, W26, W28, W30, W32, W34, W36, W38, W4, W40, Y23, Y3	GND	Ground

3 Electrical Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect conditions that the APQ8016 device may be exposed to beyond the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can be expected only within the operating conditions, as described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_A1	Analog circuits	-0.30	1.56	V
VDD_A2	Analog circuits	-0.30	2.16	V
VDD_APC	Application microprocessors	-0.30	1.62	V
VDD_CORE	Digital core circuits	-0.30	1.55	V
VDD_MEM	On-chip memory	-0.30	1.55	V
VDD_MIPI_DSI_PLL	Power for MIPI_DSI PHY PLL	-0.30	2.16	V
VDD_P1	Digital pad circuits	-0.30	1.44	V
VDD_P2	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P3	Digital pad circuits	-0.30	2.16	V
VDD_P4	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P5	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P6	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P7	Digital pad circuits	-0.30	2.45	V

Parameter		Min	Max	Unit
VDD_PLL1	PLL circuits	-0.30	1.55	V
VDD_PLL2	PLL circuits	-0.30	2.16	V
VDD_QFPROM_PRG	QFPROM programming voltage	-0.30	2.16	V
VDD_USBPHY_1P8	USB PHY low-voltage circuit	-0.30	2.16	V
VDD_USBPHY_3P3	USB PHY high-voltage circuit	-0.30	3.63	V
VDD_USB_HS	Core circuits for USB	-0.30	1.55	V
VDD_WLAN	WLAN ADC circuits	-0.30	1.56	V
Signal pins				
V_IN	Voltage on any non-power input pin	-0.3	V_{xx} + 20% [1]	V
VIN_P7	Voltage on any eMMC input pin	-0.30	2.45	V
I_IN	Latch-up current	-100	100	mA
ESD protection – see Section 7.1				
Thermal conditions – see Section 4.5				

1. VXX is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the design team: power-supply voltage, power-distribution impedances, and thermal conditions (Table 3-3). The APQ8016 meets all performance specifications listed in Section 3.3 through Section 3.12 when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for APC and CORE rails [1]

Parameter		Min	Typ	Max	Unit
VDD_APC	Quad Cortex A53 (operating at a maximum frequency of 1.15+ GHz)				
	▪ Turbo mode[3]	1.07	–	1.42	V
	▪ Nominal mode	0.97	–	1.22	V
	▪ SVS mode[2]	0.97	1.05	1.12	V
VDD_CORE	▪ Turbo mode[3]	1.05	–	1.36	V
	▪ Nominal mode	0.93	–	1.22	V
	▪ SVS mode	0.84	–	1.12	V

[1] Parts with voltages outside the specified ranges are not guaranteed to operate properly

[2] AVS type I is not enabled on the APC rail in SVS mode

[3] APQ8016 supports voltage rail scaling to save power according to dynamic system performance requirements. Turbo mode is used to enable critical system busses such as the core CPUS, the Graphics core, and the memory bus interface to reach peak frequency operational targets as required by system loading.

Table 3-3 Operating conditions

Parameter		Min	Typ [2]	Max	Unit
Power-supply voltages					
VDD_A1 VDD_WLAN	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits Power for WLAN ADC circuits	1.25	1.3	1.35	V
VDD_MEM VDD_PLL1 VDD_USB_HS	Power supply for internal memory cores Power for PLL circuits – low voltage Power for USB core circuits ▫ Turbo mode[3] ▫ Nominal mode ▫ SVS mode	 1.22 1.10 1.00	 1.2875 1.15 1.05	 1.33 1.19 1.09	 V V V
VDD_PLL2 VDD_A2 VDD_USBPHY_1P8	Power for PLL circuits – high voltage Power for analog circuits – high voltage for analog baseband receiver and SVideo circuits Power for USB PHY interface – low voltage	1.72	1.80	1.93	V
VDD_P1 VDD_MIPI	Power for pad group 1 – EBI pads Power for MIPI circuits (CSI and DSI)	1.15	1.20	1.25	V
VDD_P2	Power for pad group 2 SDC2 pads low voltage SDC2 pads high voltage	 1.67 2.75	 1.8 2.95	 1.93 3.04	 V V
VDD_P3	Power for pad group 3 – most I/O pads	1.67	1.8	1.93	V
VDD_P4	Power for pad group 4 UIM3 pads low voltage UIM3 pads high voltage	 1.67 2.75	 1.8 2.95	 1.93 3.04	 V V
VDD_P5	Power for pad group 5 UIM1 pads low voltage UIM1 pads high voltage	 1.67 2.75	 1.8 2.95	 1.93 3.04	 V V
VDD_P6	Power for pad group 6 UIM2 pads low voltage UIM2 pads high voltage	 1.67 2.75	 1.8 2.95	 1.93 3.04	 V V
VDD_P7	Power for pad group 7 – SDC1 pads	1.67	1.8	1.93	V

Parameter		Min	Typ [2]	Max	Unit
VDD_MIPI_DSI_PLL	Power for MIPI_DSI PHY PLL	1.72	1.8	1.95	V
VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise ground	1.67	1.8	1.93	V
VDD_USBPHY_3P3	Power for USB PHY interface – high voltage	2.97	3.08	3.50	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
T_A [1]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

[1] These temperature ranges are defined by the 3GPP2 system specification.

[2] Typical voltages represent the recommended output settings of the companion PMIC device.

[3] APQ8016 supports voltage rail scaling to save power according to dynamic system performance requirements. Turbo mode is used to enable critical system busses such as the core CPUS, the Graphics core, and the memory bus interface to reach peak frequency operational targets as required by system loading.

3.2.1 Core voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. These fuses are used by software. The fuse locations in Table 3-4 refer to register 0x0005C00C SECURITY_CONTROL_CORE_QFPROM_CORR_PTE2.

Table 3-4 Core voltage in retention mode

VDD_CORE	Bit 7 (MSB)	Bit 6	Bit 5 (LSB)
0.65 V	0	0	0
0.5 V	0	0	1
0.65 V	0	1	1

3.3 Power delivery network specification

This section covers the power delivery network (PDN) maximum impedance specification.

3.3.1 PDN system specification (PCB + baseband IC)

Table 3-5 lists the PCB + baseband IC PDN requirements. Meeting this specification requires the use of a commercial circuit simulator program (e.g., ADS) and the APQ8016 S-parameter model.

Table 3-5 PCB + baseband IC PDN impedance vs. frequency

Power domain	Required PCB routing inductance (caps shorted) [1]	Max impedance		
		DC to 10 Hz	10 Hz to 10 MHz	10–500 MHz
VDD_MEM	500 pH max.	11 mΩ	104 mΩ	250 mΩ
VDD_CORE	250 pH	5 mΩ	79 mΩ	160 mΩ
VDD_APC	200 pH	4 mΩ	45 mΩ	140 mΩ

[1] Meeting the PCB routing inductance is the required starting point to reap maximum benefits from the PDN capacitor optimization process.

3.3.2 PDN specification (PCB-only)

Table 3-6 lists the PCB-only PDN requirements. Refer to this specification **only** if a commercial circuit simulator program (e.g., ADS) is not available.

Table 3-6 PCB-only PDN impedance vs. frequency

Power domain	Max impedance		Pin number of positive ports	Pin number of negative ports
	DC to 10 Hz	10 Hz to 25 MHz		
VDD_MEM	11 mΩ	78 mΩ	All VDD_MEM pins	All GND pins
VDD_CORE	5 mΩ	78 mΩ	All VDD_CORE pins	All GND pins
VDD_APC	4 mΩ	45 mΩ	All VDD_APC pins	All GND pins
VDD_P1	35 mΩ	141 mΩ	J10, J14, K11	G10, G12, G14, G16, K9, J16
		141 mΩ	J20, J22	G18, G20, G24, J18, K21
		141 mΩ	J24, K23	G24, K21
		141 mΩ	K15, K19	K17, K21
		141 mΩ	J30	G28, G30, G32, J32

NOTE: The PDN DC specification for VDD_P1 applies for both APQ and external memory domains powered by VREG_L2_1P2 under the assumption that the maximum current drawn by memory device is 250 mA. The PDN AC specification for VDD_P1 applies only for APQ domain powered by VREG_L2_1P2.

3.4 DC power characteristics

3.4.1 Dhrystone and rock bottom maximum power

Table 3-7 lists values for Dhrystone and rock bottom power specifications.

Table 3-7 Dhrystone and rock bottom power specifications

APQ version	Dhrystone (W) at 85°C (T_j) [1 2 3]	Rock bottom (mW) at 25°C (T_j) [3]
APQ8016 (1.15+ GHz)	3.78	11.8

1 Dhrystone should be measured using the QTI custom Dhrystone script that will be provided upon request.

2 The Dhrystone specification applies only to APQ8016 CS devices. Dhrystone should be run and measured on all four cores together.

3 Rock bottom (VDD_CORE and VDD_MEM) should be measured at VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at retention voltage.

3.5 Power sequencing

The PM8916 includes poweron circuits that provide the proper power sequencing for the entire APQ8016 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins.

A high-level summary of the required poweron sequence:

- VDD_MEM (on-chip memory), VDD_PLL1
- VDD_CORE (digital core circuits)
- VDD_APC (Cortex A53 microprocessor)
- VREF_SDC (SDC reference voltage)
- VDD_P3 (I/Os), VDD_P7 (SDC1), VDD_DDR_1P8
- VDD_USBPHY_1P8, VDD_PLL2
- VDD_P1 (EBI and DDR I/Os), VDD_DDR_1P2
- VREG_XO
- EBI0_VREF_XX (LPDDR2/3 reference voltage)
- VDD_USB_3P3
- VDD_QFPROM_PRG, VDD_P2 (SDC2)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_Px), so that internal circuits can take control of the I/Os and pads.
- If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.
- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_Ax), since the SSBIs are initialized to their default states before VDD_Ax powers up (analog circuits are controlled by SSBI).

- Other non-critical supplies are included within the poweron sequence. Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_MEM reaches 90% of its value, then the VDD_CORE supply can start ramping up.

3.6 Digital logic characteristics

A digital I/O's performance specification depends upon its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the APQ8016 and other ICs within the chipset, and therefore do not require specification.
- Some are defined by existing standards (such as I^2C, SPI, etc). This device complies with those standards and additional specifications are not required.
- All other digital I/Os require performance specifications, and are organized within this section as described in Table 3-8.

Table 3-8 Digital I/Os specified in this section

Pad voltage	Usage	Table
1.2 V	EBI0 (P1)	Table 3-9
1.8 V	GPIO (P3)	Table 3-10
Dual- V (1.8 V/2.95 V)	SDC2 (P2), GPIO (P5, P6, P4), UIM1 (P5), UIM2 (P6), UIM3 (P4)	Table 3-11
Dual- V (1.2 V/1.8 V)	SDC1(P7)	Table 3-12

Table 3-9 1.2 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
EBI0 pads only (as identified in Table 3-8)					
V_{REF}	Reference voltage		0.49 * V_{DD_Px}	0.51 * V_{DD_Px}	V
V_{IH}	High-level input voltage	CMOS/Schmitt	V_{REF} + 0.13	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	V_{REF} - 0.13	V
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA

Parameter		Comments	Min	Max	Unit
I_{IHPD}	Input high leakage current with pull-down		40	200	µA
I_{ILPU}	Input low leakage current with pull-up		-200	-40	µA
I_{OZHKP}	High-level, tri-state leakage current with keeper		-120	-10	µA
I_{OZLKP}	Low-level, tri-state leakage current with keeper		10	120	µA
V_{OH}	High-level output voltage	CMOS, at rated drive strength[1]	0.9 * V_{DD_Px}	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[1]	–	0.1 * V_{DD_Px}	V
$C_{I/O}$	I/O capacitance[2]		1.25	2.50	pF

[1] Refer to Table 2-1 for each output pin's drive strength (IOH and IOL); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
[2] Input capacitance and I/O capacitance values are guaranteed by design, but not 100% tested.

Table 3-10 1.8 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
GPIO (P3) (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_Px}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength[1]	V_{DD_Px} - 0.45		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[3]	–	0.45	V
R_P	Pull resistance[2]	Pull-up and pull-down	55	390	kΩ
R_K	Keeper resistance[2]		30	150	kΩ
I_{IH}	Input high leakage current[3]	No pull-down	–	1	µA
I_{IL}	Input low leakage current[4]	No pull-up	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	I/O capacitance		–	5	pF

Parameter		Comments	Min	Max	Unit
RFFE & SPMI pins					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	0.8 * V_{DD_PX}		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.2 * V_{DD_Px}	V
R_P	Pull resistance	Pull-up and pull-down	10	50	kΩ
R_K	Keeper resistance		10	50	kΩ
I_{IH}	Input high leakage current	No pull-down	–	1	µA
I_{IL}	Input low leakage current	No pull-up	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		165	–	mV

1 Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.

2 Refer to Table 2-1 for pull-up, pulldown, and keeper options for each pad (where appropriate).

3 Pad voltage = V_{DD_Px} max.

4 Over all valid pad voltages.

Table 3-11 Dual-voltage 1.8 V/2.95 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
Common to dual-voltage pads 1.8 V/2.95 V (as identified in Table 3-8)					
R_P	Pull resistance[1]	Pull-up and pull-down	10	100	kΩ
R_K	Keeper resistance[1]		10	100	kΩ
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	IO capacitance		–	5	pF
Common to SDC2 pad and UIM pad at 2.95 V only (as identified in Table 3-8)					
I_{IH}	Input high leakage current	No pull-down	–	10	µA
I_{IL}	Input low leakage current	No pull-up	-10	–	µA

Parameter		Comments	Min	Max	Unit
Common to UIM pads, either voltage (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.7 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.2 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength[2]	0.8 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[2]	0	0.4	V
SDC2 pads at 2.95 V only (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.25 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength [2]	0.75 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[2]	0	0.125 * V_{DD_Px}	V
Common to SDC2 pad and UIM pad at 1.8 V only (as identified in Table 3-8)					
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA
SDC2 pads at 1.8 V only (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	1.27	2	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.58	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.4		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	0	0.45	V

[1] Refer to Table 2-1 for pull-up, pull-down, and keeper options for each pad (where appropriate).
[2] Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.

Table 3-12 Dual-voltage 1.2 V/1.8 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
Common to all dual-voltage pads 1.2 V / 1.8 V					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_Px}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA
R_P	Pull resistance[1]	Pull-up and pull-down	10	100	kΩ
R_K	Keeper resistance[1]		10	100	kΩ
C_{IN}	Input capacitance		–	5	pF
SDC1 (P7) pad at 1.2 V only					
V_{OH}	High-level output voltage	CMOS, at rated drive strength	0.75 * V_{DD_Px}	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.25 * V_{DD_Px}	V
SDC1 (P7) pad at 1.8 V only					
V_{OH}	High-level output voltage	CMOS, at rated drive strength	V_{DD_Px} - 0.45	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.45	V

[1] Refer to Table 2-3 for pull-up, pull-down, and keeper options for each pad (where appropriate).

In all digital I/O cases, V_{OL} and V_{OH} are linear functions with respect to the drive current (given in Table 2-3). They can be calculated using the relationships expressed in Figure 3-1.

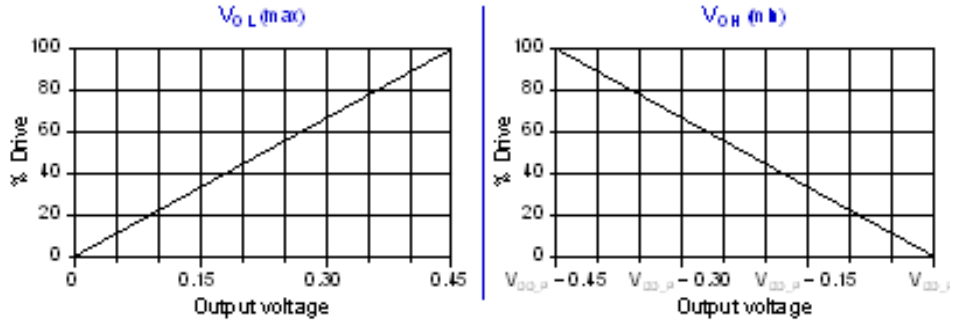


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_Px})

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad-design methodologies are included here.

NOTE: All APQ8016 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This discussion is described further in Section 3.7.2.

3.7.1 Timing-diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

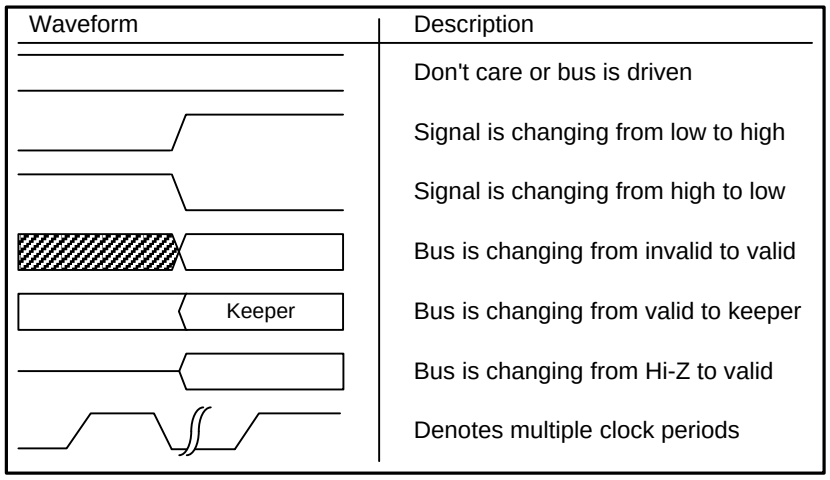


Figure 3-2 Timing-diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus-type signal (multiple bits) – the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal – indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize APQ8016 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

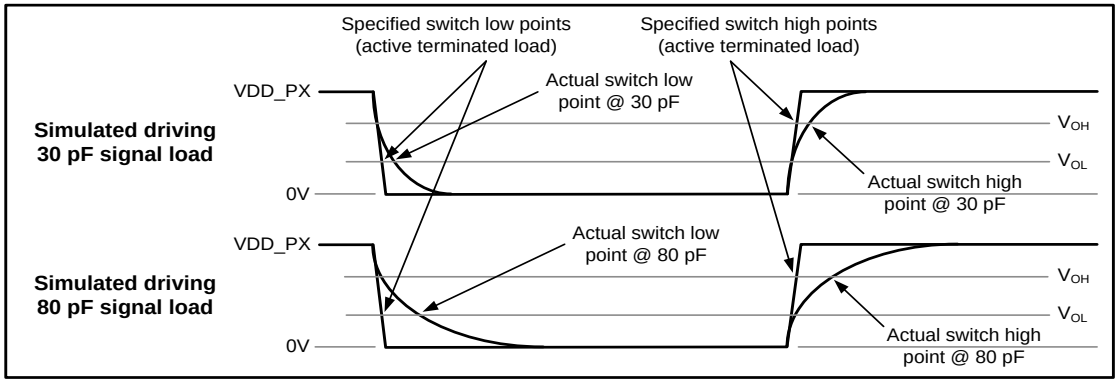


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the APQ device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

NOTE: Board designers should use the relevant APQ8016 IBIS File for this analysis.

3.7.3 Pad design

The APQ8016 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_Px} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_Px}/2$ (or 50% of V_{DD_Px}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_Px} for V_{IL} and 65% of V_{DD_Px} for V_{IH}.

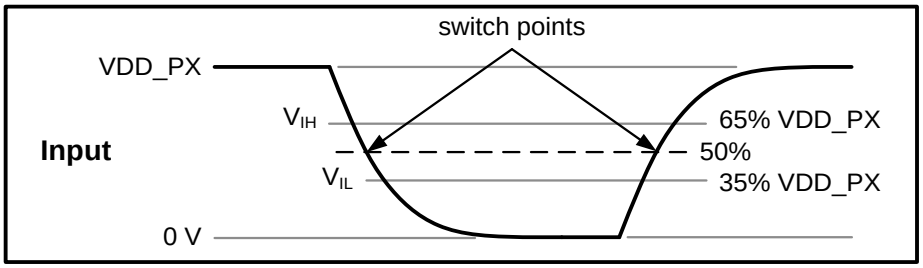


Figure 3-4 Digital input signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that may have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be as follows:

- V_{OH} ~ VDD_Px - 50 mV or more
- V_{OL} ~ 50 mV or less

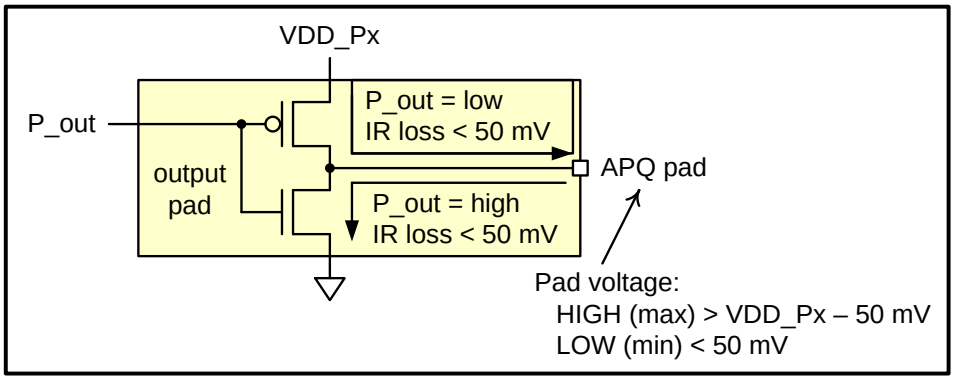


Figure 3-5 Output-pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_Px} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_Px} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will get worse and hold-time numbers may get better.

3.8.1 EBI0 memory support

The APQ8016 EBI0 port supports an external LPDDR2/3 SDRAM memory:

- Interface frequency of up to 533 MHz
- 1.2V IO interface

3.8.1.1 EBI0 pad drive strength

Pads for EBI0 are tailored for its 1.2 V interface and are source-terminated. Before the source termination, the pad drive strength is 15 mA to 60 mA. But at the pads, after the source termination, the drive strength at IOL, IOH is equivalent to 0.90 mA to 3.35 mA in nonlinear steps when the JEDEC standard range (90% – 10%) is followed.

3.8.1.2 LPDDR2/3 SDRAM clock

For any timing analysis, the measurement point for all signals is at 50% of VDD_Px. All output timing parameters represent the point of the output signal transition; additional accounting for signal rise and fall times for specific bus loading is required.

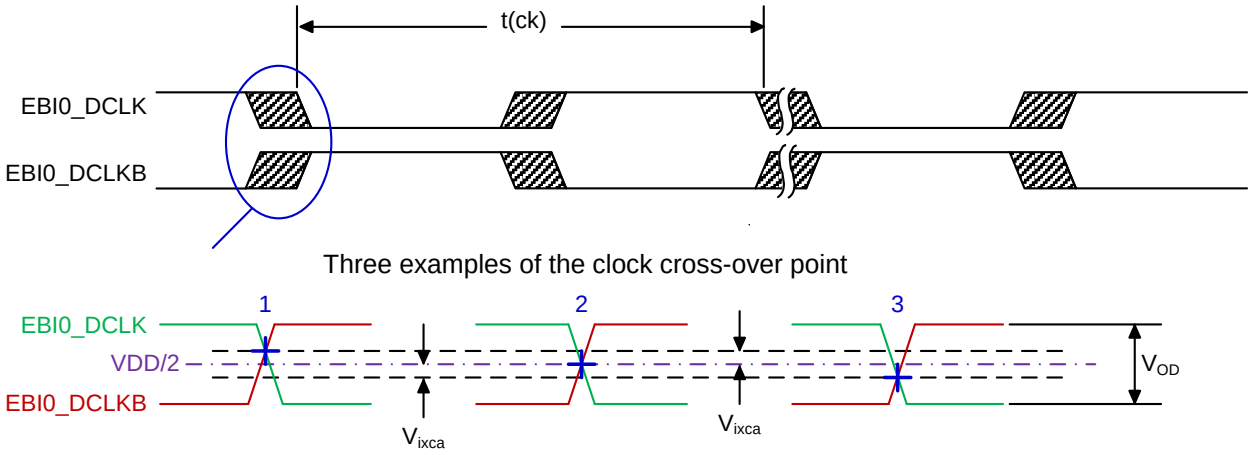


Figure 3-6 DDR SDRAM DCLK and DCLKB

Table 3-13 DDR SDRAM clock-timing parameters

Parameter		Comments	Min	Typ	Max	Unit
$1/t_{CK}$	DDR clock frequency		10	–	533 (LPDDR2) 533 (LPDDR3)	MHz
	Duty cycle		45	–	55	%
V_{ixca}[1]	Clock crossover-point	± offset from VDD/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

[1] Crosstalk due to high CA activity might cause parameters to exceed the V_{ixca} limit.

3.8.1.3 LPDDR2/3 SDRAM strobe

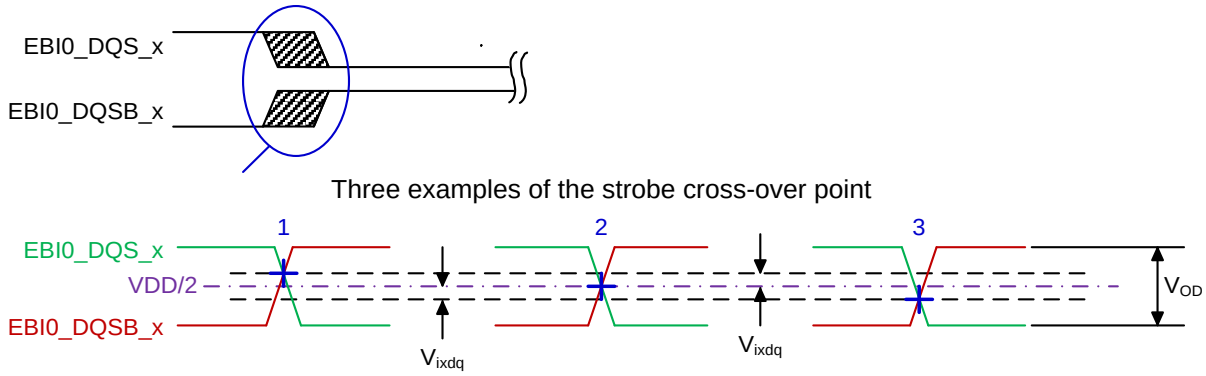


Figure 3-7 DDR SDRAM DQS_x and DQSB_x

Table 3-14 DDR SDRAM strobe timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock cross-over point	± offset from VDDQ/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

3.8.1.5 LPDDR2 SDRAM read and write timing

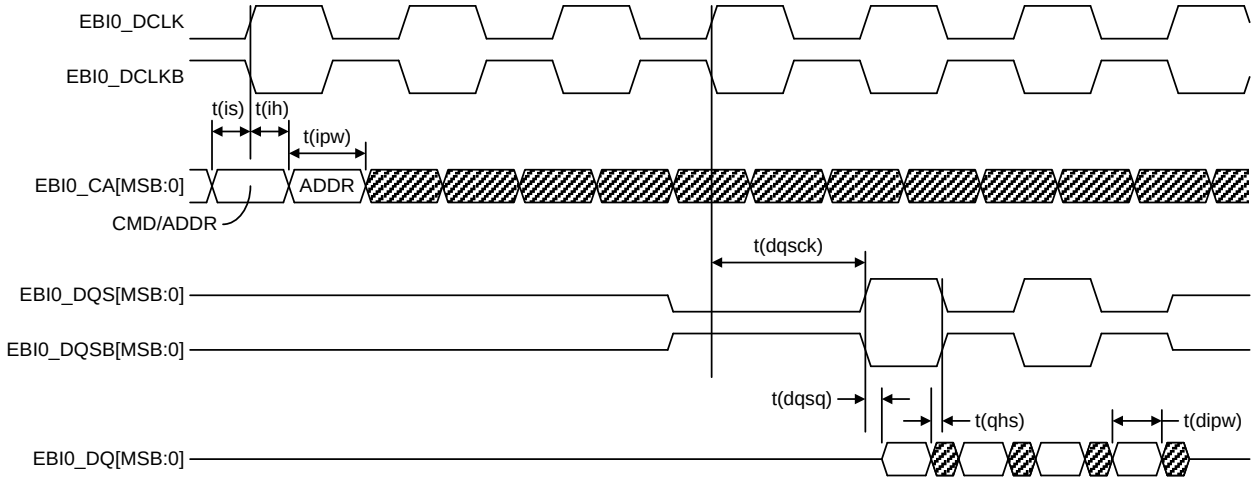


Figure 3-8 LPDDR2 SDRAM read timing diagram

Table 3-15 LPDDR2 SDRAM read timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR2 (533 MHz) – common to read and write						
t(is)	Address & control in setup time before CK		0.22	–	–	ns
t(ih)	Address & control input hold time after CK		0.22	–	–	ns
t(dipw)	DQ & DM pulse width		0.35	–	–	tCK
t(ipw)	Address & control input pulse width		0.40	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR2 (533 MHz) – read cycle						
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns
t(dqsq)	DQS to DQ skew limit		–	–	0.2	ns
t(rpre)	Read preamble		0.90	–	–	t(ck)
t(qhs)	Data hold skew factor		–	–	0.23	ns

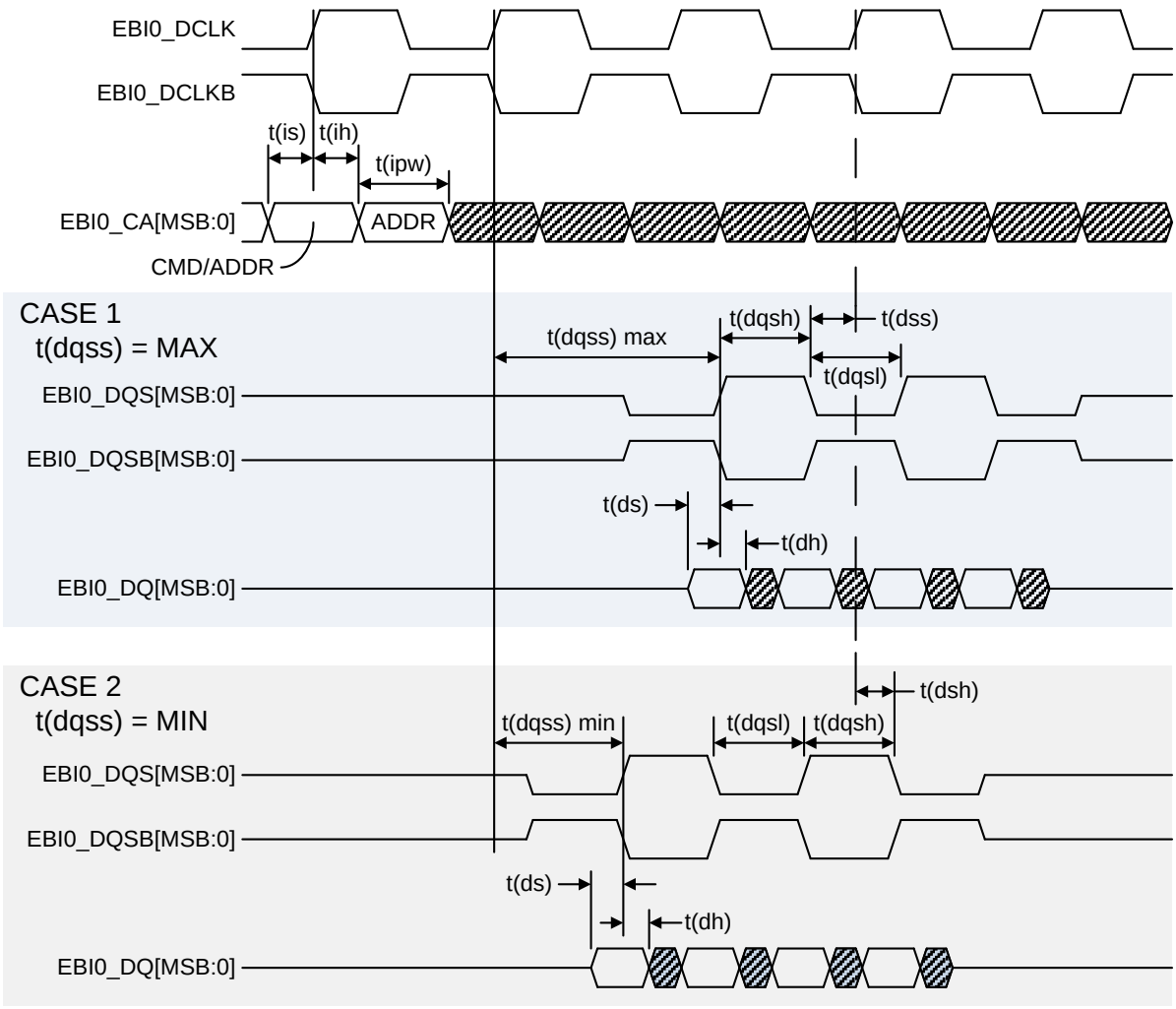


Figure 3-9 LPDDR2 SDRAM write timing diagram

Table 3-16 LPDDR2 SDRAM write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR2 (533 MHz) – common to read and write						
t(is)	Address & control in setup time before CK		0.22	–	–	ns
t(ih)	Address & control input hold time after CK		0.22	–	–	ns
t(dipw)	DQ & DM pulse width		0.35	–	–	tCK
t(ipw)	Address & control input pulse width		0.40	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR2 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.21	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.21	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.20	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.20	–	–	t(ck)

3.8.1.6 LPDDR3 SDRAM read and write timing

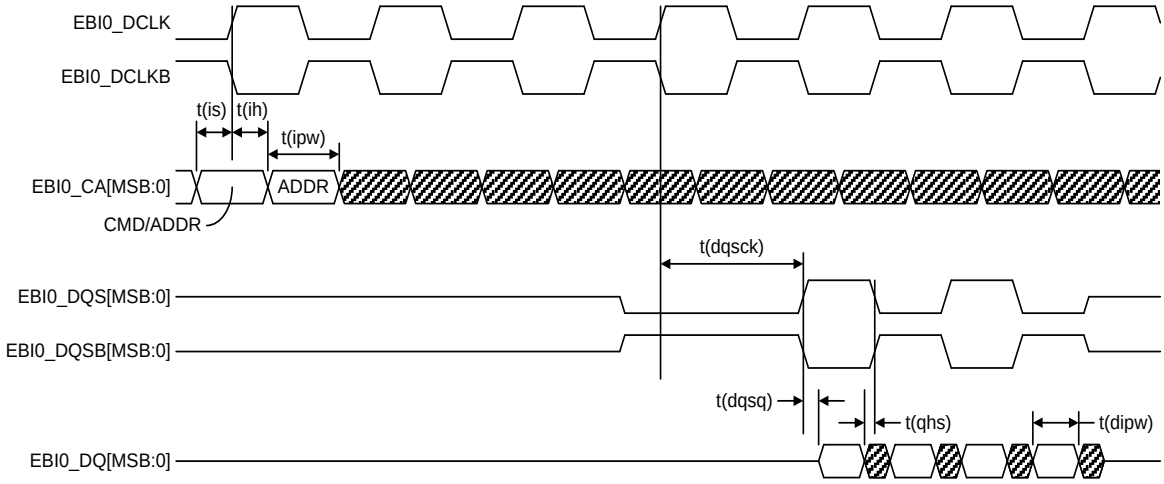


Figure 3-10 LPDDR3 SDRAM read timing diagram

Table 3-17 LPDDR3 SDRAM read timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – common to read and write						
t(isca)	Address & control in setup time before CK		0.175	–	–	ns
t(ihca)	Address & control input hold time after CK		0.175	–	–	ns
t(dipw)	DQ & DM pulse width		0.35	–	–	t(ck)
t(iscs)	CS_n input setup time		0.29	–	–	ns
t(ihcs)	CS_n input hold time		0.29	–	–	ns
t(ipwcs)	CS_n input pulse width		0.7	–	–	t(ck)
t(ipw)	Address & control input pulse width		0.35	–	–	t(ck)
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR3 (533 MHz) – read cycle						
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns
t(dqsq)	DQS to DQ skew limit		–	–	0.165	ns
t(qhs)	Data hold skew factor		–	–	0.713	ns
t(rpre)	Read preamble		0.9	–	–	t(ck)

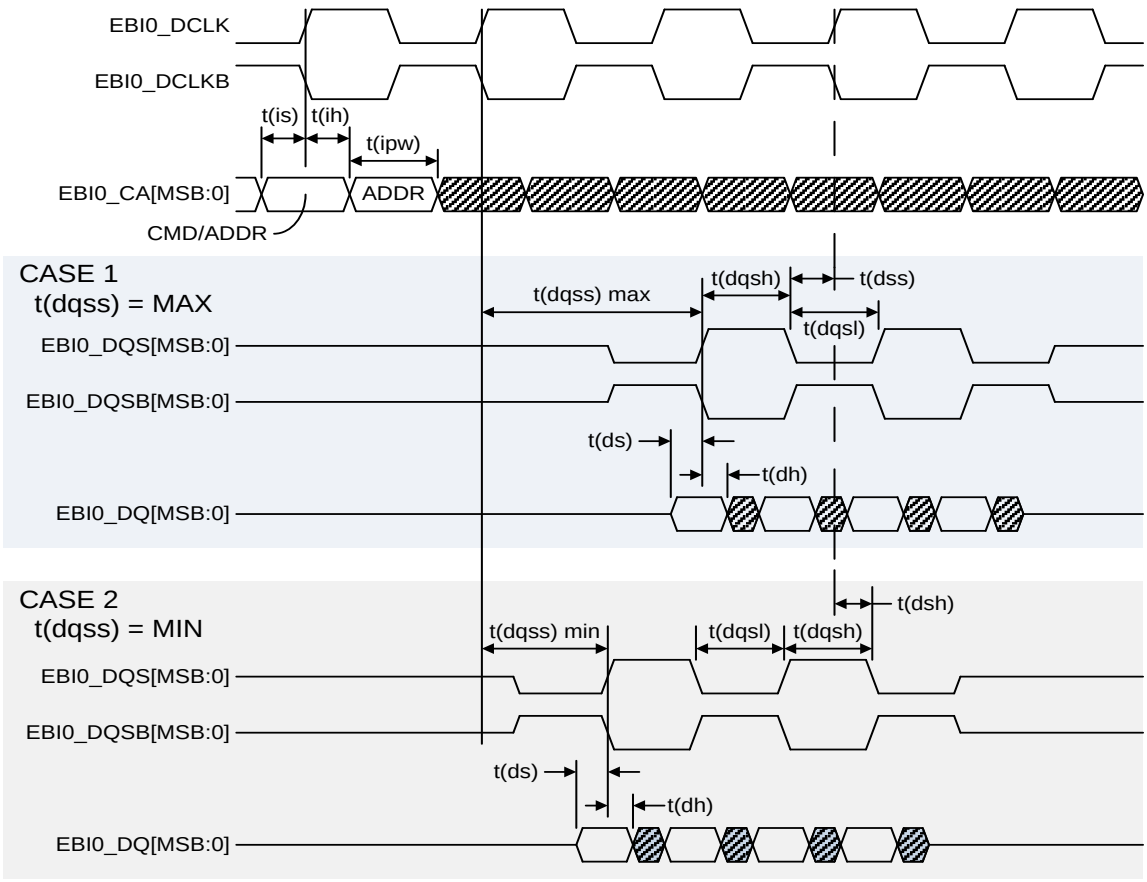


Figure 3-11 LPDDR3 SDRAM write timing diagram

Table 3-18 LPDDR3 SDRAM write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – common to read and write						
t(isca)	Address & control in setup time before CK		0.175	–	–	ns
t(ihca)	Address & control input hold time after CK		0.175	–	–	ns
t(dipw)	DQ & DM pulse width		0.35	–	–	t(ck)
t(iscs)	CS_n input setup time		0.29	–	–	ns
t(ihcs)	CS_n input hold time		0.29	–	–	ns
t(ipwcs)	CS_n input pulse width		0.7	–	–	t(ck)
t(ipw)	Address & control input pulse width		0.35	–	–	t(ck)
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.175	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.175	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.2	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.2	–	–	t(ck)

3.8.2 eMMC on SDC1

See Section 3.10.1 for secure digital interface details.

3.9 Multimedia

Multimedia parameters that require performance specification are addressed in this section.

3.9.1 Camera interfaces

The APQ8016 supports two MIPI_CSIs:

- CSI0 is a single 4-lane CSI
- CSI1 is a 2-lane CSI

Table 3-19 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for D-PHY, v0.65 and v0.9/v1.0, October 8, 2007 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	Supports only unidirectional data receiving.	None

3.9.2 Audio support

The APQ8016 device provides the system's audio functions with the analog audio codec integrated into PM8916 device. A proprietary audio PDM interface through GPIO[63:68] was used for transmission of audio data with PM8916 integrated analog codec.

APQ audio-related audio interfaces that support other audio devices included:

- I^2S – Section 3.10.3
- I^2C – Section 3.10.4

3.9.3 Display support

The APQ8016 supports a 4-lane MIPI_DSI.

Table 3-20 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification v1.01 for Display Serial Interface http://www.mipi.org/specifications/display-interface (Specifications are available to MIPI members only.)	None	None
MIPI D-PHY Specification v0.65, v0.81, v0.90 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	None	None

3.10 Connectivity

The connectivity functions supported by the APQ8016 device that require electrical specifications include:

- Secure digital (SD), including SD cards and multimedia cards (MMC)
- Universal serial bus (USB)
- Inter-IC sound (I^2S) interfaces
- Inter-integrated circuit (I^2C) interfaces
- Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are included in the following subsections.

NOTE: In addition to reviewing the following hardware specifications, also be sure to review the latest software release notes for software-based performance features or limitations.

3.10.1 Secure digital interfaces

Table 3-21 Supported SD standards and exceptions

Applicable standard	Feature exceptions	Device variations
Multi Media Card Host Specification, version 4.5.1	None	Timing specifications – see Figure 3-12 and Table 3-22
Secure Digital: Physical Layer Simplified Specification, version 3	None	
SDIO Card Specification, version 2.0 https://www.sdcard.org/downloads/pls/simplified_specs/archive/partE1_200.pdf (Simplified specification version 3.00 is available for free download.)	None	

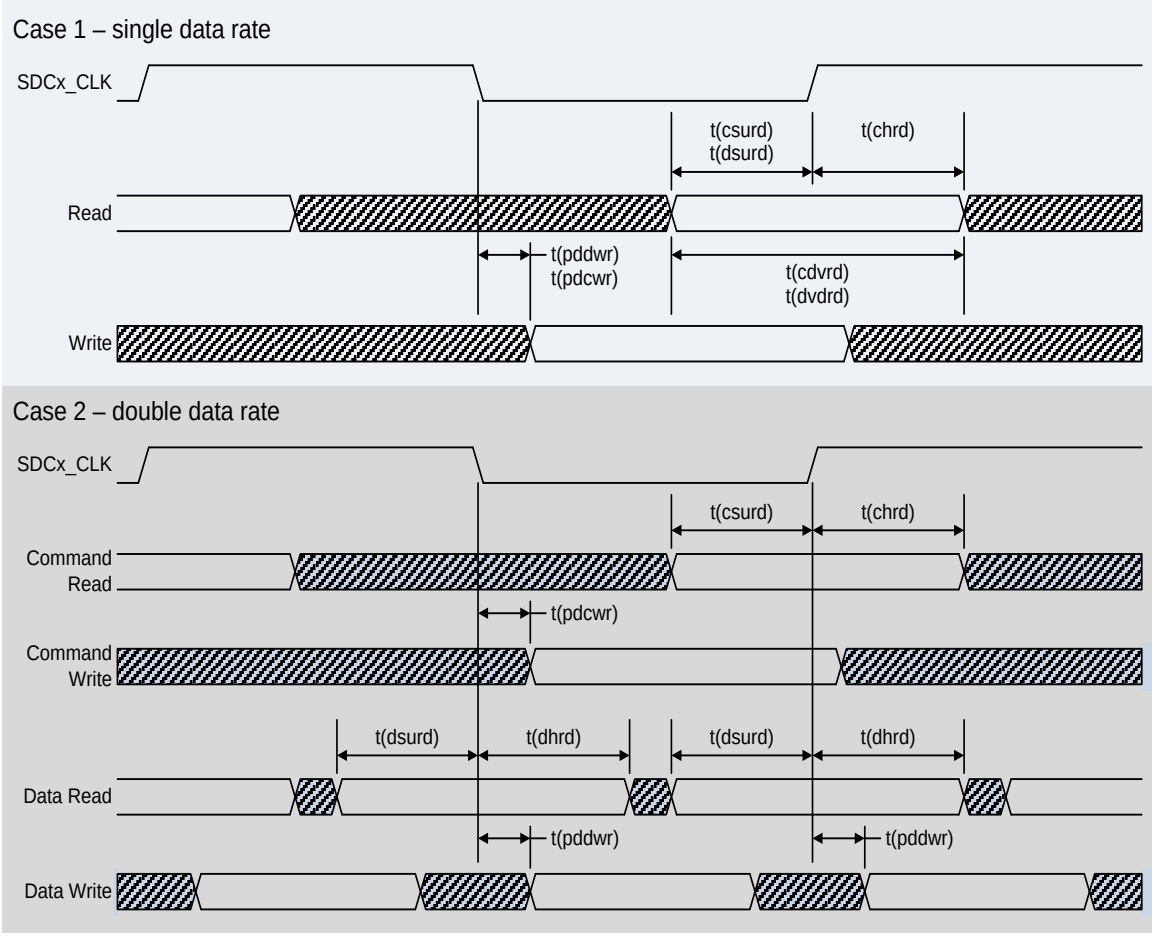


Figure 3-12 Secure digital interface timing diagram

Table 3-22 Secure digital interface timing specifications

Parameter		Min	Typ	Max	Unit
Single data rate (SDR) mode – SDC1 up to 200 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.45	–	0.85	ns
t(pdcwr)	Propagation delay on command write	-1.45	–	0.85	ns
Double data rate (DDR) mode – SDC1 up to 52 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	5.53	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	1.65	–	–	ns
t(pddwr)	Propagation delay on data write	2.5	–	6.15	ns
t(pdcwr)	Propagation delay on command write	-7.85	–	2.65	ns
SDR mode – SDC2 up to 208 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.36	–	0.76	ns
t(pdcwr)	Propagation delay on command write	-1.36	–	0.76	ns
DDR mode – SDC2 up to 50 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	6.3	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2	–	–	ns
t(pddwr)	Propagation delay on data write	0.8	–	6	ns
t(pdcwr)	Propagation delay on command write	-8.2	–	3	ns

Parameter		Min	Typ	Max	Unit
SDR mode – SDC2 up to 100 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	2.5	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2.5	–	–	ns
t(pddwr)	Propagation delay on data write	-3.7	–	1.5	ns
t(pdcwr)	Propagation delay on command write	-3.7	–	1.5	ns

3.10.2 USB interfaces

Table 3-23 Supported USB standards and exceptions

Applicable standard	Feature exceptions	Device variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later) http://www.usb.org/developers/docs/ (Available for free download.)	None	Operating voltages, system clock, and VBUS – see Table 3-24
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0A or later) http://www.usb.org/developers/docs/ (Available for free download as part of the USB 2.0	Supports host mode aspect of OTG only	None

Table 3-24 Device-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 3-3 for specifications) VDD_USB_1P8 VDD_USB_3P3		 – –	 1.80 3.075	 – –	 V V
USB_SYSCLK					
Frequency	19.2 MHz clock is required	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	ps

Parameter	Comments	Min	Typ	Max	Unit
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.85	V
High-level input voltage (V_{IH})		1.27	–	–	V
USB_VBUS					
Valid USB_HS_VBUS detection voltage		2.00	–	5.25	V

3.10.3 I²S interface

The MI²S (multiple I²S) interface for microphone and speaker functions is supported by APQ8016. MI²S is a multichannel I²S. The standard I²S specifications defined by Philips consists of one data line and our I²S interface adds one or more data lines and thus it is called MI²S. Protocol is the same as I²S and with MI²S, but more audio channels can be supported. The following information applies to MI²S.

Table 3-25 Supported I²S standards and exceptions

Applicable standards	Feature exceptions	APQ variations
Phillips I²S Bus Specifications revised June 5, 1996 https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf (Available for free download.)	1. Only the *normal* I²S format is supported: data is transmitted on the falling edge of clock and latched at rising edge 2. Only 16, 23, and 32- bit modes are supported 3. I²S IOs are 1.8V nominal, 2.0V max	When an external SCK clock is used, a duty cycle of 45% to 55% is required.

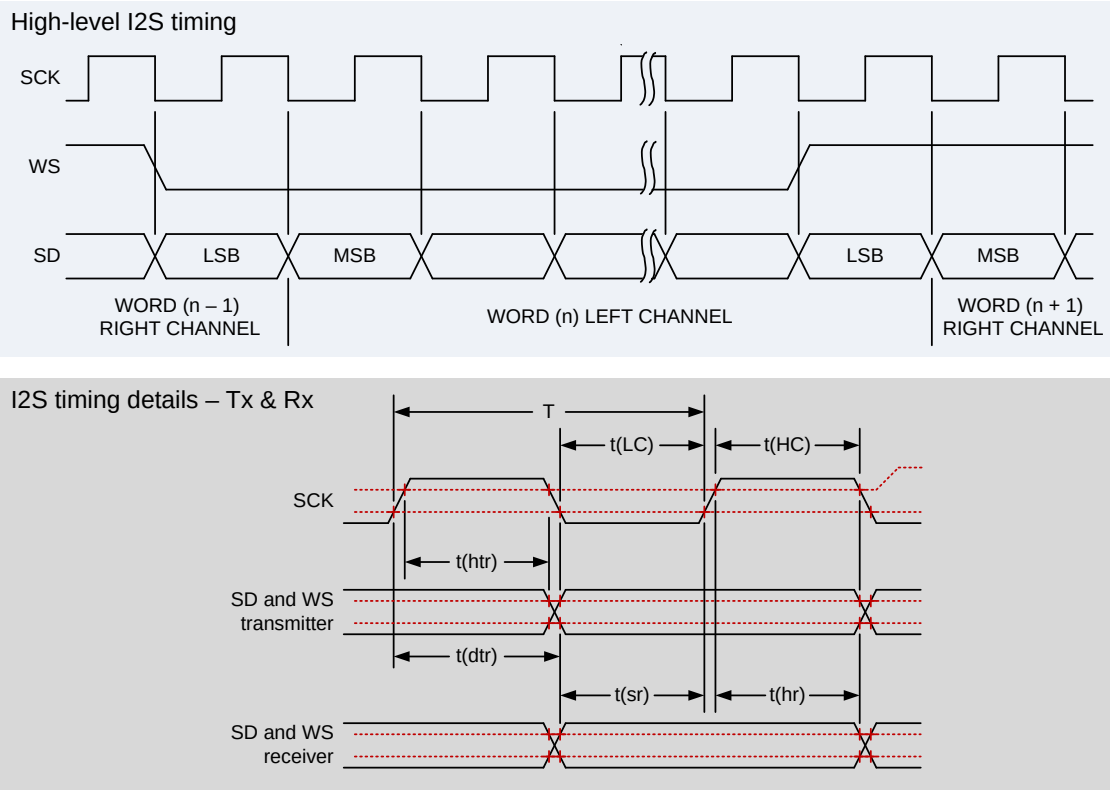


Figure 3-13 I²S timing diagram

Table 3-26 I²S interface timing

Parameter		Comments[1]	Min	Typ	Max	Unit
Using internal SCK						
	Frequency		–	–	12.288[2]	MHz
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns
Using external SCK						
	Frequency		–	–	12.288	MHz

Parameter		Comments[1]	Min	Typ	Max	Unit
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns

[1] Load capacitance is between 10 and 40 pF.

[2] 12.288 MHz is the maximum I²S interface frequency, but the actual frequency used is programmable and depends on the number of bits and sampling rate desired.

3.10.4 Digital microphone PDM interface

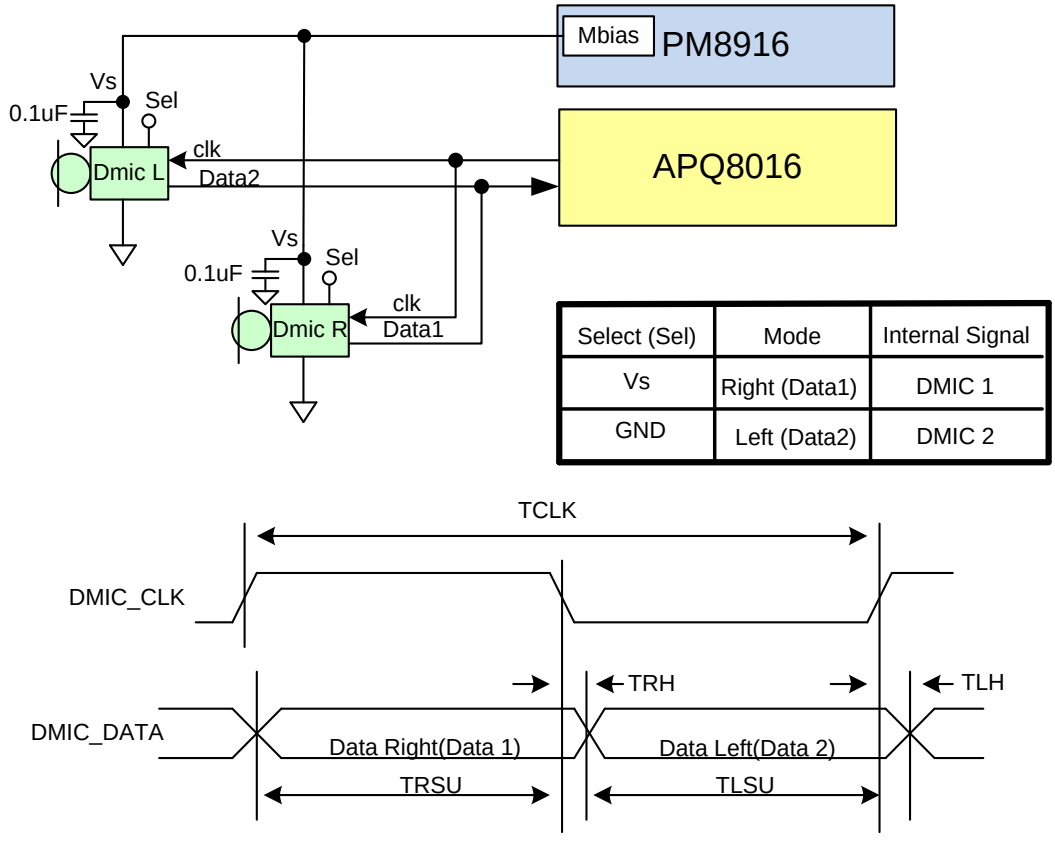


Figure 3-14 APQ8016 digital mic PDM interface timing

Table 3-27 Digital microphone timing

Parameter	Min	Type	Max	Unit
DMIC clock period (T_{CLK})	163	–	1666	ns
Data left setup time to DMIC clock rising edge (T_{LSU})	30	–	–	ns
Data left hold time from DMIC clock rising edge (T_{LH})	5	–	–	ns
Data right setup time to DMIC clock falling edge (T_{RSU})	30	–	–	ns
Data right hold time from DMIC clock falling edge (T_{RH})	5	–	–	ns

Table 3-28 Digital microphone input path performance for sampling rates of 8 kHz, 16 kHz, 32 kHz, and 48 kHz

Parameter	Conditions	Min	Type	Max	Units
Frequency response					
Frequency response	Passband: 20 Hz to 0.4*Fs; digital gain = 0 dB; input = -20 dBFs	-0.01	0	0.01	dB
	Transition band 1: 0.4* Fs to 0.4375* Fs; digital gain = 0 dB; input = -20 dBFs	-1	–	0.1	dB
	Transition band 2: 0.5*Fs; digital gain = 0 dB; input = -20 dBFs	-25	–	–	dB
	Stopband: >0.5625*Fs; digital gain = 0 dB; input = -20 dBFs	-80	–	–	dB
General requirements					
Clock rate	MCLK = 9.6 MHz (Default system master clock frequency)	–	600	–	kHz
		–	1.2	–	MHz
		–	2.4	–	MHz
		–	3.2	–	MHz
		–	4.8	–	MHz
	MCLK = 12.288 MHz	–	768	–	kHz
		–	1.536	–	MHz
		–	2.048	–	MHz
		–	3.072	–	MHz
		–	4.096	–	MHz
		–	6.144	–	MHz
Input capacitance		–	1	5	pF

Parameter	Conditions	Min	Type	Max	Units
Board capacitance		–	10	50	pF

3.10.5 I²C interface

Table 3-29 Supported I²C standards and exceptions

Applicable standard	Feature exceptions	APQ variations
I²C Specification, version 5.0, October 2012	1. Slave mode is not supported 2. 10-bit addressing is not supported 3. Multi-master is not supported 4. HS mode is not supported	Multimaster is not supported

3.10.6 Serial peripheral interface

The APQ8016 supports SPI as a master only. Any one of the six BLSP ports can be configured as an SPI master. Figure 3-15 is an example of BLSP @ 50 MHz (see Table 3-30).

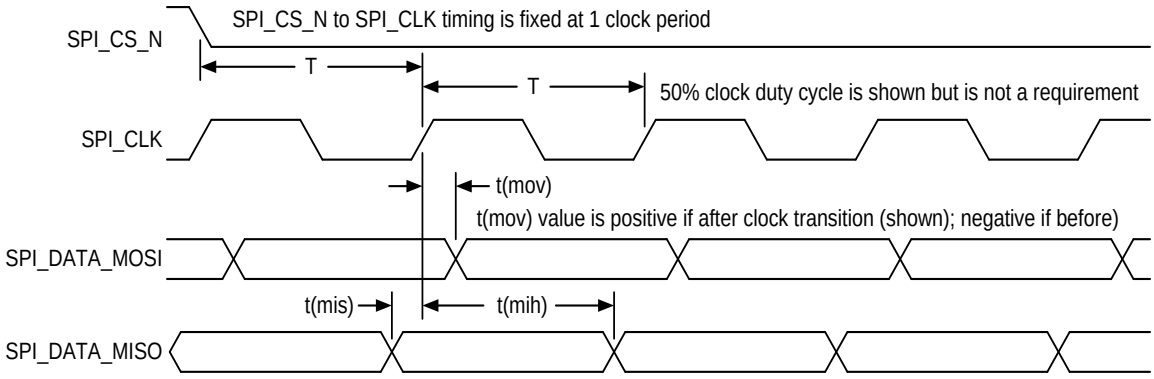


Figure 3-15 SPI master timing diagram

Table 3-30 SPI master timing characteristics at 50 MHz

Parameter	Comments	Min	Typ	Max	Unit
T[1]	SPI clock period: 50 MHz max	20.0	–	–	ns
t(ch)	Clock high	9.0	–	–	ns
t(cl)	Clock low	9.0	–	–	ns
t(mov)	Master output valid	-5.0	–	5.0	ns

Parameter	Comments	Min	Typ	Max	Unit
t(mis)	Master input setup	5.0	–	–	ns
t(mih)	Master input hold	1.0	–	–	ns

[1] The minimum clock period includes 1% jitter of the maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified in the following subsections.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here in this section.

3.11.1.1 19.2 MHz XO input

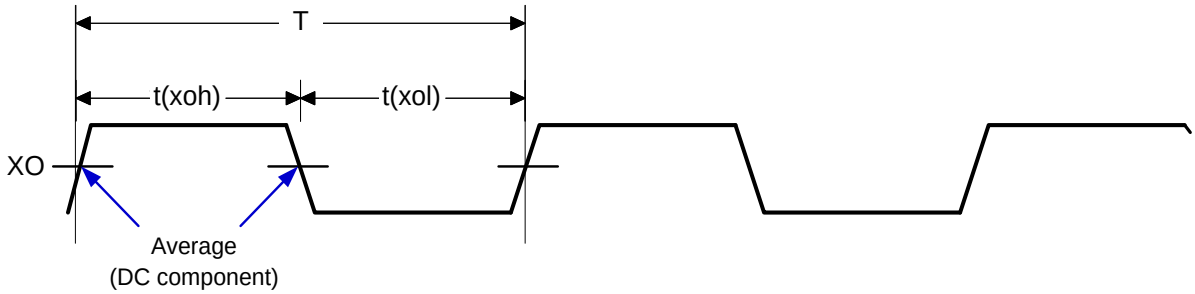


Figure 3-16 XO timing parameters

Table 3-31 XO timing parameters

Parameter		Comments[1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

[1] See *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH + Xtal Mini-Specification* (LM80-P0598-8) for more details.

3.11.1.2 Sleep clock

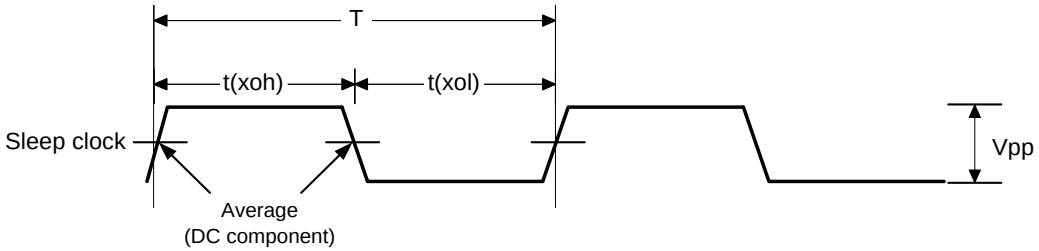


Figure 3-17 Sleep-clock timing diagram

Table 3-32 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T	Sleep-clock period		–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

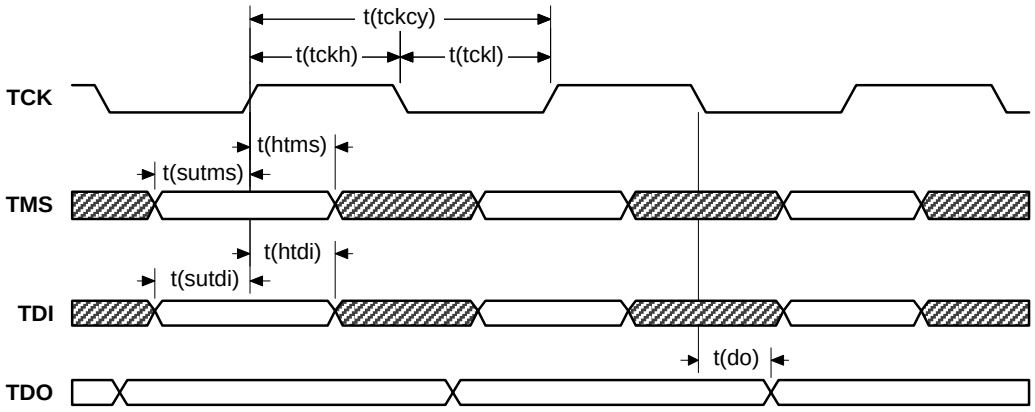


Figure 3-18 JTAG-interface timing diagram

Table 3-33 JTAG-interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data-output delay		–	–	15	ns

3.12 RF and power management interfaces

The supported chipset and RF front-end (RFFE) interfaces are listed in Table 3-34 and Table 3-35, respectively. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 RF front-end (RFFE)

Table 3-34 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for RF Front-End Control Interface, version 1.0	None	None

The maximum operation frequency of SCLK is 26 MHz, although lower rates may be utilized. A Slave might not be able to support a 26 MHz clock frequency during a read operation. In this case, known as half-speed operation, a 13 MHz clock frequency may be implemented for only the read back.

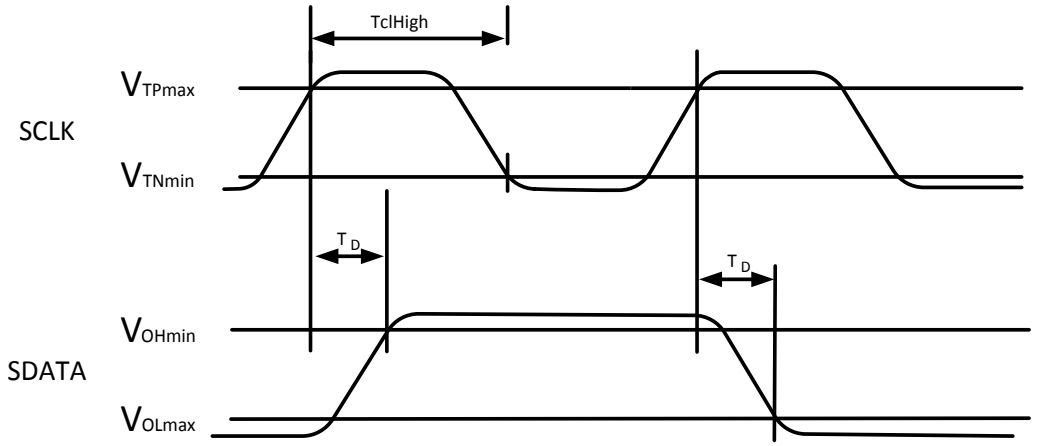


Figure 3-18 Waveform

Table 3-35 RFFE data

Symbol	Description	Half speed device		Full speed device		Units
		Min	Max	Min	Max	
Tsclkoh	Clock output high time	24		11.25		ns
Tsclkol	Clock output low time	24		11.25		ns
Tsclkotr	Clock output transition (rise/fall) time 1	3.5	10	3.5	6.5	ns
Tsclkdch	Clock output duty cycle high time 2, 3	45	55	45	55	ns
Tsclkdcl	Clock output duty cycle low time 2, 3	45	55	45	55	ns

Table 3-36 Rx/Tx data

Parameter	Description	LSL	USL	units
Tsu	Rx data setup time with respect to falling edge of clock	15.75	–	ns
Thd	Rx data hold time with respect to falling edge of clock	0	–	ns
Tpd	Tx data output delay w.r.to rising edge of clock	NA	10.25	ns
TclHigh	Tx clock duty cycle	0.45*Tck	0.55*Tck	ns

3.12.2 System power management interface (SPMI)

Table 3-37 SPMI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

Table 3-38 Supported SPMI standards

Interface	Parameter	Description	Target frequency	Spec min	Spec max	Units
SPMI	Tsu	Input data set up time	19.2 MHz	1	1	ns
	Thd	Input data hold time		5	5	ns
	TdataZ	data release time		-	11	ns
	Tpd	Output data delay		-	11	ns

4 Mechanical Information

4.1 Device physical dimensions

The APQ8016 is available in the 760-pin nanoscale package (NSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 760 NSP has a 14.0 mm × 12.0 mm body with a maximum height of 0.96 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 760NSP outline drawing is shown in Figure 4-1.

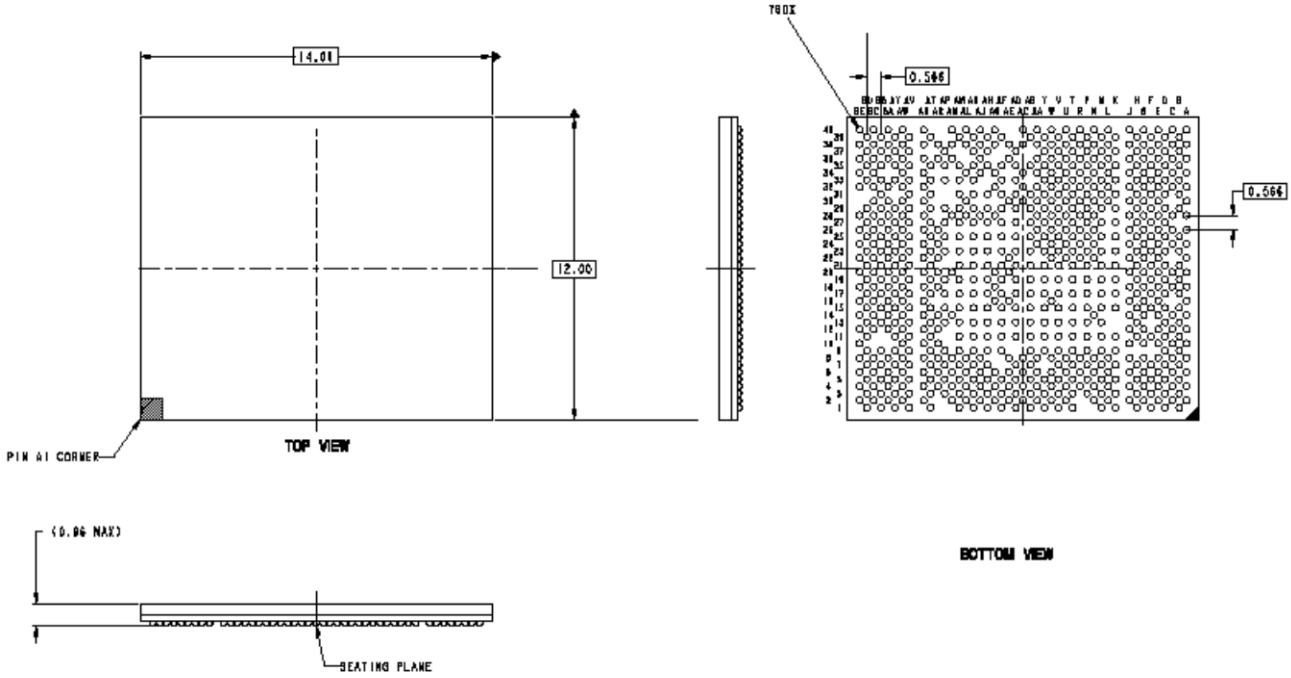


Figure 4-1 760 NSP (14.0 × 12.0 × 0.96 mm) outline drawing

NOTE: Figure 4-1 is a simplified outline drawing.

4.2 Part marking

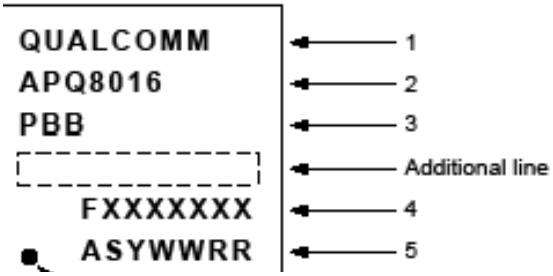


Figure 4-2 APQ8016 device marking (top view, not to scale)

4.2.1 Specification-compliant devices

Table 4-1 APQ8016 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	APQ8016	QTI product name
3	PBB	P = product configuration code (see Table 4-2) BB = feature code (see Table 4-2)
An additional line may appear on the part marking for some samples; this is manufacturing information that is only relevant to QTI and QTI suppliers.		
4	FXXXXXXX	F = supply source code ■ F = A (for GF) ■ F = B (for TSMC) ■ F = C (for Samsung) XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ A = U (Amkor, Shanghai) ■ A = K (SPIL Taiwan) ■ A = V (STATSChipPAC, China) ■ A = E (ASE, Kaohsiung, Taiwan) S = assembly sequence number Y = single-digit year code WW = work week (based on calendar year) RR = product revision (see Table 4-2)

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained in this section.

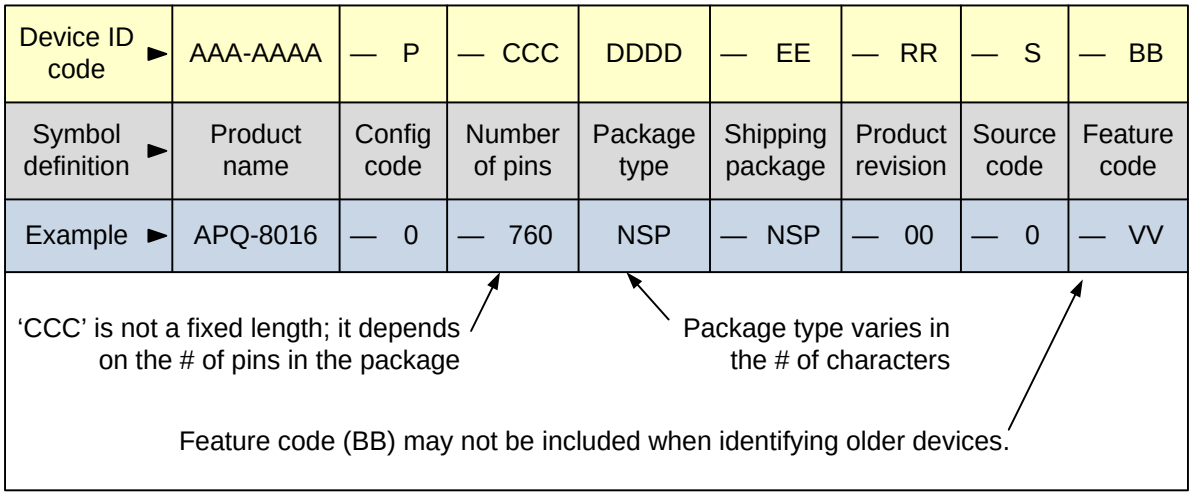


Figure 4-3 APQ8016 device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (*P*)	Product revision (*RR*)	HW revision number	Sample type	HW version	S value[1]	BB value[2]
APQ-8016	1	00	0x0 0706 0E1	ES/CS	v1.0	0	VV

[1] "S" is the source configuration code that identifies all of the qualified die fabrication-source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-3.

[2] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. All feature sets available at the time of this document's release are defined in Table 4-2.

NOTE: Devices with date code (YWW) = 1423 or later are CS devices.

Table 4-3 Source configuration code

S value	Die	F value = A	F value = B	F value = C
0	Digital	GF	TSMC	Samsung
Other columns and rows will be added in future revisions of this document, if needed.				

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-4.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be re-flowed within the time limit specified on the label.	≤ 30°C/60% RH

The latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification are followed. ***The APQ8016 device samples are currently classified as MSL3 at 255 (+5, -0)°C***. This qualification temperature (255 (+5, -0)°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal-package models are provided through the CDMATech Support website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can obtain thermal resistance values by conducting their own thermal simulations.

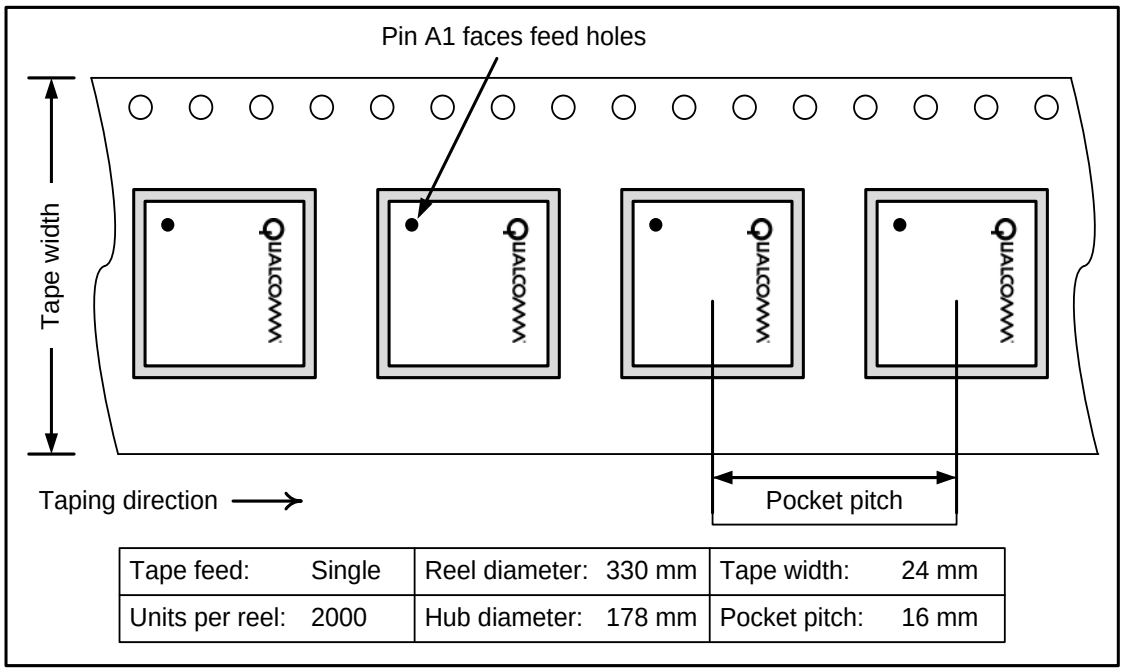
5 Carrier, Storage, & Handling Information

5.1 Carrier

5.1.1 Tape and reel information

All carrier tape systems conform to EIA-481 standards.

A simplified sketch of the APQ8016 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2 Tape handling.

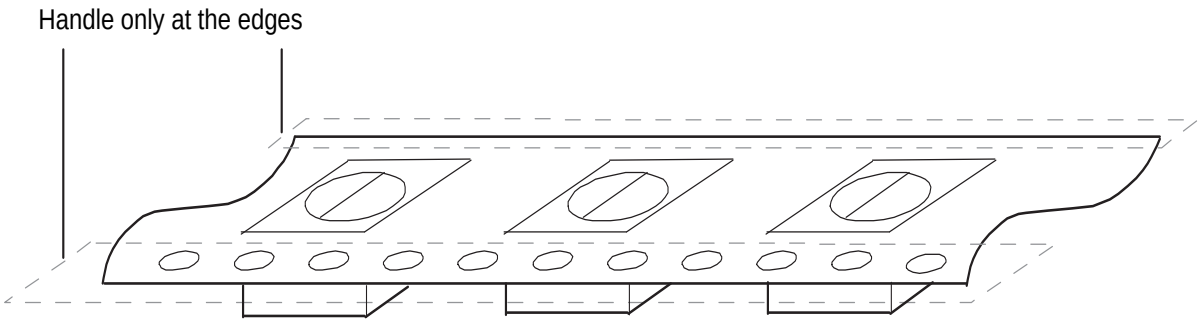


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

APQ8016 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. If the storage environment maintains an ambient temperature lower than 40°C and relative humidity less than 90%, the expected shelf life is at least 24 months.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following sections.

5.3.1 Baking

It is **not necessary** to bake the APQ8016 if the conditions specified in Section 5.2.1 and Section 5.2.2 **not been exceeded**.

It is **necessary** to bake the APQ8016 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

This product must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the APQ8016 device ESD ratings.

6 PCB Mounting Guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC305 composition on the top and SAC125/Ni on the bottom. Lead-free (or Pb-free) semiconductor products are defined as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

Characterization of the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production is recommended. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). Square apertures are recommended for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

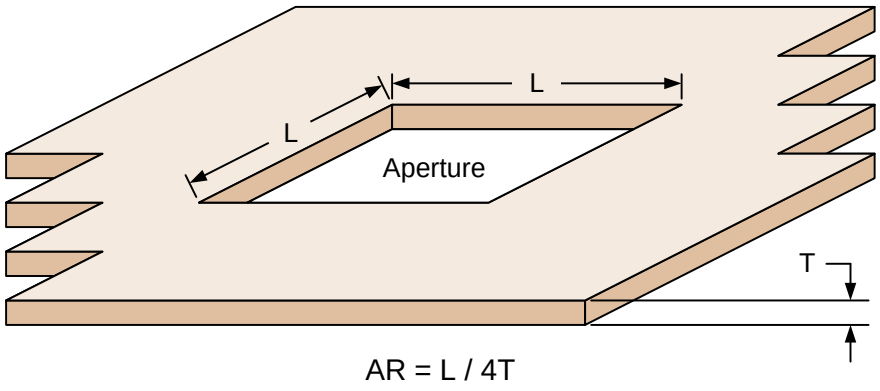


Figure 6-1 Area ratio (AR)

Example Land Pattern and stencil designs are available for the 760 NSP.

6.2.2 Reflow profile

Reflow profile conditions typically used for lead-free systems are listed in Table 6-1, and are shown in Figure 6-2.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

[1] During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

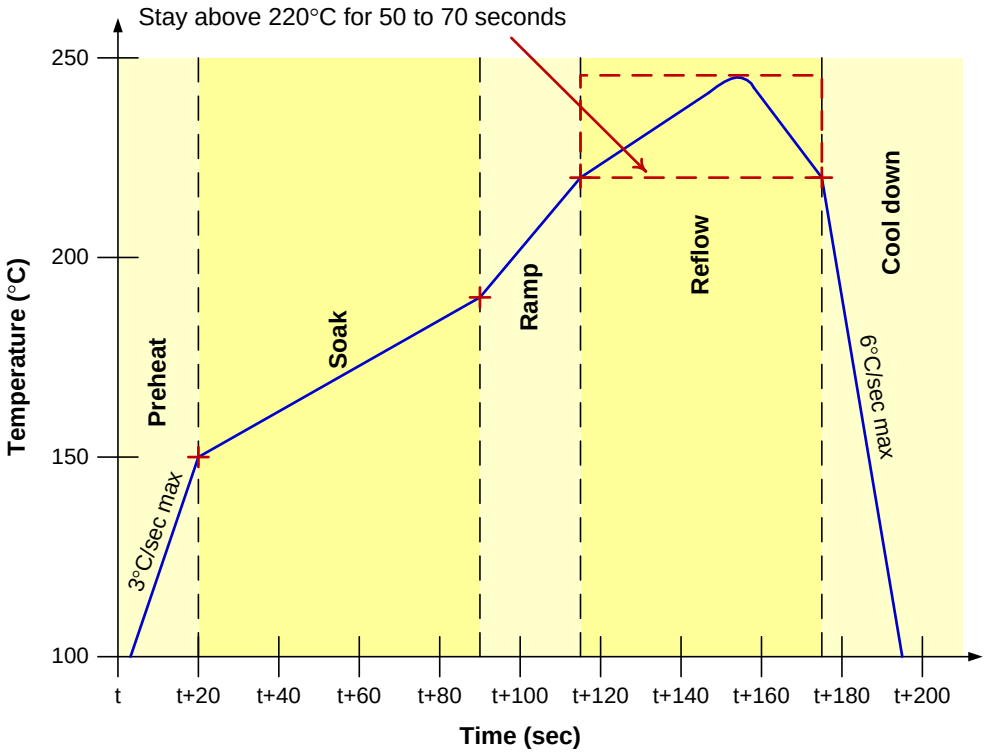


Figure 6-2 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in two other places within this document; without explanation, they may appear to conflict. The two places are listed below, along with an explanation of the stated value and its meaning within that section's context.

- Section 4.4 – *Device moisture-sensitivity level*

  APQ8016 devices are classified as MSL3@255°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained immediately below.

- Section 6.2.2– *Reflow profile*

  During a production board's reflow process, the temperature experienced by the package must be controlled. Obviously the temperature must be high enough to melt the solder and provide reliable connections, but it must not be so high that the device can be damaged. The recommended peak temperature during production assembly is 245°C. This temperature is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

6.2.4 SMT process verification

Verification of the SMT process is recommended prior to high-volume board assembly, including the following:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Board-level reliability

Characterization tests have been conducted to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

7 Part Reliability

7.1 Reliability evaluation summary

7.1.1 APQ8016 reliability evaluation report for device from GF-F8

Table 7-1 GF-F8 silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	0F/356	DPPM < 1000 [1] Cum FITs < 25 FITs[1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	0F/356	> 40 [1]
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply over-voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{dd} max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

[1] Cum FITs from multiple products under GF F8, 28 nm LP process.

Table 7-2 GF-F8 package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours. duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	135 [1]	135 [1]	135 [2]	135 [1]	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours. Total samples from three different assembly lots at each SAT	240	240	240	240	Pass

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Flammability **Note**: flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mount are rated V-0 (better than V-1).	–	–	–	–	
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

[1] Data is bridged from the 488 NSP 12 x 12 mm package.

[2] Data is bridged from the 745 PNSP 12 x 12 mm package.

7.1.2 APQ8016 reliability evaluation report for device from TSMC-F15

Table 7-3 TSMC-F15 silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	0F/360	DPPM < 1000 [1] Cum FITs < 25 FITs [1]
Mean time to failure (MTTF) t = $1/\lambda$ in million hours Total samples from three different wafer lots	0F/360	> 40 [1]
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V

Tests, standards, and conditions	Sample size	Result
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply over-voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{dd} max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

[1] Cum FITs from multiple products under TSMC-F15, 28 nm LP process.

Table 7-4 TSMC-F15 package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes. Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots at each SAT	135[1]	135 [1]	135 [2]	135 [1]	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability **Note**: Flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mount are rated V-0 (better than V-1).	–	–	–	–	
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

[1] Data is bridged from the 488 NSP 12 x 12 mm package.

[2] Data is bridged from the 745 PNSP 12 x 12 mm package.

7.1.3 APQ8016 reliability evaluation report for device from Samsung

Table 7-5 Samsung silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	456	DPPM < 1000 [1] Cum FITs < 25 FITs [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	456	> 40 [1]
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85C Total samples from one wafer lot	6	Pass
Latch-up (V supply over-voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

[1] Cum FITs from multiple products under the Samsung, 28 nm LP process.

Table 7-6 Samsung package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes. Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	135[1]	135 [1]	135[2]	135 [1]	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability **Note**: Flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mount are rated V-0 (better than V-1).	–	–	–	–	

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

[1] Data is bridged from the 488 NSP 12 x 12 mm package.
[2] Data is bridged from the 745 PNSP 12 x 12 mm package.

7.2 Qualification sample description

Table 7-7 Device characteristics

Device	Specifications
Device name	APQ8016
Package type	760 NSP
Package body size	14 mm × 12 mm × 0.96 mm
Fab process	28 nm CMOS
Fab sites	▪ GF ▪ TSMC ▪ Samsung
Assembly sites	▪ Amkor, Shanghai ▪ SPIL, Taiwan ▪ STATSChipPAC, China ▪ ASE, Kaohsiung, Taiwan
Solder ball pitch	0.4 mm

8 EXHIBIT 1

PLEASE READ THIS LICENSE AGREEMENT ("AGREEMENT") CAREFULLY. THIS AGREEMENT IS A BINDING LEGAL AGREEMENT ENTERED INTO BY AND BETWEEN YOU (OR IF YOU ARE ENTERING INTO THIS AGREEMENT ON BEHALF OF AN ENTITY, THEN THE ENTITY THAT YOU REPRESENT) AND QUALCOMM TECHNOLOGIES, INC. ("QTI" "WE" "OUR" OR "US"). THIS IS THE AGREEMENT THAT APPLIES TO YOUR USE OF THE DESIGNATED AND/OR ATTACHED DOCUMENTATION AND ANY UPDATES OR IMPROVEMENTS THEREOF (COLLECTIVELY, "MATERIALS"). BY USING OR COMPLETING THE INSTALLATION OF THE MATERIALS, YOU ARE ACCEPTING THIS AGREEMENT AND YOU AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. IF YOU DO NOT AGREE TO THESE TERMS, QTI IS UNWILLING TO AND DOES NOT LICENSE THE MATERIALS TO YOU. IF YOU DO NOT AGREE TO THESE TERMS YOU MUST DISCONTINUE AND YOU MAY NOT USE THE MATERIALS OR RETAIN ANY COPIES OF THE MATERIALS. ANY USE OR POSSESSION OF THE MATERIALS BY YOU IS SUBJECT TO THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT.

1.1 **License**. Subject to the terms and conditions of this Agreement, including, without limitation, the restrictions, conditions, limitations and exclusions set forth in this Agreement, Qualcomm Technologies, Inc. ("QTI") hereby grants to you a nonexclusive, limited license under QTI's copyrights to use the attached Materials; and to reproduce and redistribute a reasonable number of copies of the Materials. You may not use Qualcomm Technologies or its affiliates or subsidiaries name, logo or trademarks; and copyright, trademark, patent and any other notices that appear on the Materials may not be removed or obscured. QTI shall be free to use suggestions, feedback or other information received from You, without obligation of any kind to You. QTI may immediately terminate this Agreement upon your breach. Upon termination of this Agreement, Sections 1.2-4 shall survive.

1.2 **Indemnification**. You agree to indemnify and hold harmless QTI and its officers, directors, employees and successors and assigns against any and all third party claims, demands, causes of action, losses, liabilities, damages, costs and expenses, incurred by QTI (including but not limited to costs of defense, investigation and reasonable attorney's fees) arising out of, resulting from or related to: (i) any breach of this Agreement by You; and (ii) your acts, omissions, products and services. If requested by QTI, You agree to defend QTI in connection with any third party claims, demands, or causes of action resulting from, arising out of or in connection with any of the foregoing.

1.3 **Ownership**. QTI (or its licensors) shall retain title and all ownership rights in and to the Materials and all copies thereof, and nothing herein shall be deemed to grant any right to You under any of QTI's or its affiliates' patents. You shall not subject the Materials to any third party license terms (e.g., open source license terms). You shall not use the Materials for the purpose of identifying or providing evidence to support any potential patent infringement claim against QTI, its affiliates, or any of QTI's or QTI's affiliates' suppliers and/or direct or indirect customers. QTI hereby reserves all rights not expressly granted herein.

1.4 **WARRANTY DISCLAIMER**. YOU EXPRESSLY ACKNOWLEDGE AND AGREE THAT THE USE OF THE MATERIALS IS AT YOUR SOLE RISK. THE MATERIALS AND TECHNICAL SUPPORT, IF ANY, ARE PROVIDED "AS IS" AND WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS OR IMPLIED. QTI ITS LICENSORS AND AFFILIATES MAKE NO WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THE MATERIALS OR ANY OTHER INFORMATION OR DOCUMENTATION PROVIDED UNDER THIS AGREEMENT, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR AGAINST INFRINGEMENT, OR ANY EXPRESS OR IMPLIED WARRANTY ARISING OUT OF TRADE USAGE OR OUT OF A COURSE OF DEALING OR COURSE OF PERFORMANCE. NOTHING CONTAINED IN THIS AGREEMENT SHALL BE CONSTRUED AS (I) A WARRANTY OR REPRESENTATION BY QTI, ITS LICENSORS OR AFFILIATES AS TO THE VALIDITY OR SCOPE OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT OR (II) A WARRANTY OR REPRESENTATION BY QTI THAT ANY MANUFACTURE OR USE WILL BE FREE FROM INFRINGEMENT OF PATENTS, COPYRIGHTS OR OTHER INTELLECTUAL PROPERTY RIGHTS OF OTHERS, AND IT SHALL BE THE SOLE RESPONSIBILITY OF YOU TO MAKE SUCH DETERMINATION AS IS NECESSARY WITH RESPECT TO THE ACQUISITION OF LICENSES UNDER PATENTS AND OTHER INTELLECTUAL PROPERTY OF THIRD PARTIES.

1.5 **LIMITATION OF LIABILITY**. IN NO EVENT SHALL QTI, QTI'S AFFILIATES OR ITS LICENSORS BE LIABLE TO YOU FOR ANY INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE, OR THE DELIVERY OR FAILURE TO DELIVER, ANY OF THE MATERIALS, OR ANY BREACH OF ANY OBLIGATION UNDER THIS AGREEMENT, EVEN IF QTI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE FOREGOING LIMITATION OF LIABILITY SHALL REMAIN IN FULL FORCE AND EFFECT REGARDLESS OF WHETHER YOUR REMEDIES HEREUNDER ARE DETERMINED TO HAVE FAILED OF THEIR ESSENTIAL PURPOSE. THE ENTIRE LIABILITY OF QTI, QTI's AFFILIATES AND ITS LICENSORS, AND THE SOLE AND EXCLUSIVE REMEDY OF YOU, FOR ANY CLAIM OR CAUSE OF ACTION ARISING HEREUNDER (WHETHER IN CONTRACT, TORT, OR OTHERWISE) SHALL NOT EXCEED US$10.

2. **COMPLIANCE WITH LAWS**; APPLICABLE LAW. You agree to comply with all applicable local, international and national laws and regulations and with U.S. Export Administration Regulations, as they apply to the subject matter of this Agreement. This Agreement is governed by the laws of the State of California, excluding California's choice of law rules.

3. **CONTRACTING PARTIES**. If the Materials are downloaded on any computer owned by a corporation or other legal entity, then this Agreement is formed by and between QTI and such entity. The individual accepting the terms of this Agreement represents and warrants to QTI that they have the authority to bind such entity to the terms and conditions of this Agreement.

4. **MISCELLANEOUS PROVISIONS**. This Agreement, together with all exhibits attached hereto, which are incorporated herein by this reference, constitutes the entire agreement between QTI and You and supersedes all prior negotiations, representations and agreements between the parties with respect to the subject matter hereof. No addition or modification of this Agreement shall be effective unless made in writing and signed by the respective representatives of QTI and You. The restrictions, limitations, exclusions and conditions set forth in this Agreement shall apply even if QTI or any of its affiliates becomes aware of or fails to act in a manner to address any violation or failure to comply therewith. You hereby acknowledge and agree that the

restrictions, limitations, conditions and exclusions imposed in this Agreement on the rights granted in this Agreement are not a derogation of the benefits of such rights. You further acknowledges that, in the absence of such restrictions, limitations, conditions and exclusions, QTI would not have entered into this Agreement with You. Each party shall be responsible for and shall bear its own expenses in connection with this Agreement. If any of the provisions of this Agreement are determined to be invalid, illegal, or otherwise unenforceable, the remaining provisions shall remain in full force and effect. This Agreement is entered into solely in the English language, and if for any reason any other language version is prepared by any party, it shall be solely for convenience and the English version shall govern and control all aspects. If You are located in the province of Quebec, Canada, the following applies: The Parties hereby confirm they have requested this Agreement and all related documents be prepared in English.