

1

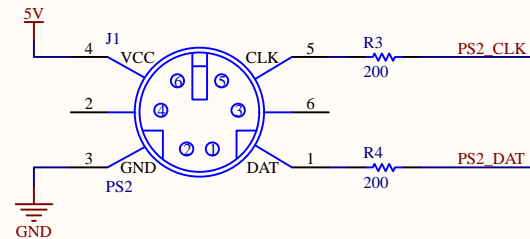
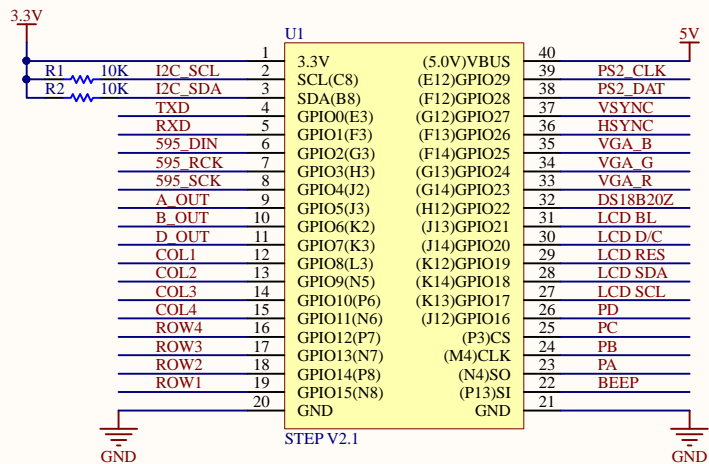
2

3

4

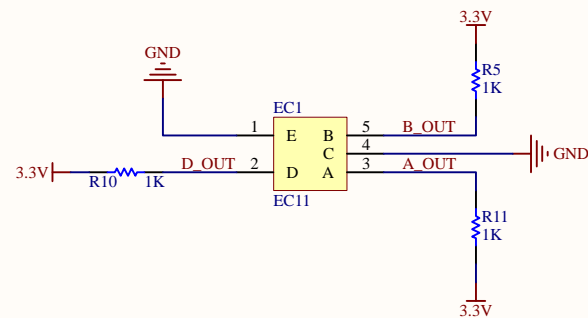
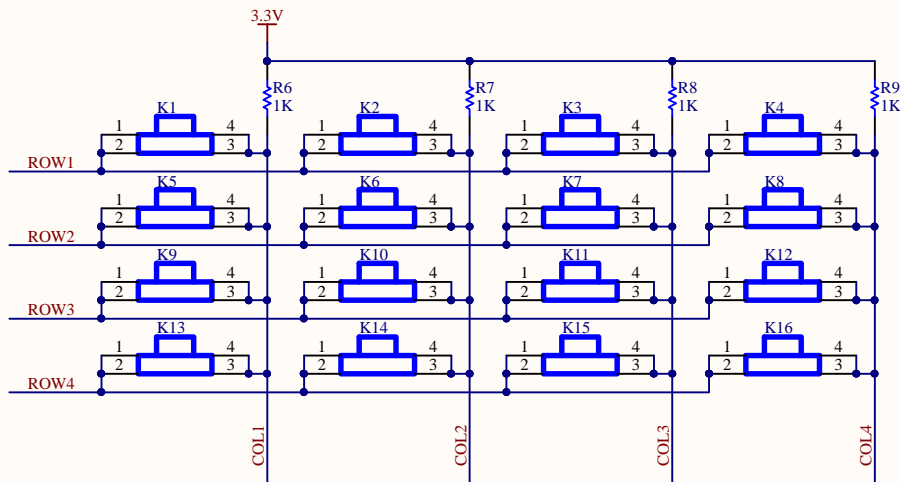
A

A



B

B



C

C

D

D

Title STEP V2.1 BaseBoard			*
Size: A4	Number:*	Revision:V2.1	*
Date: 2017/5/27	Time: 10:23:30	Sheet 1 of 3	*
File: F:\PCB_Project\STEP V2.1 BaseBoard_003\STEP V2.1 BaseBoard_1.SchDoc			*

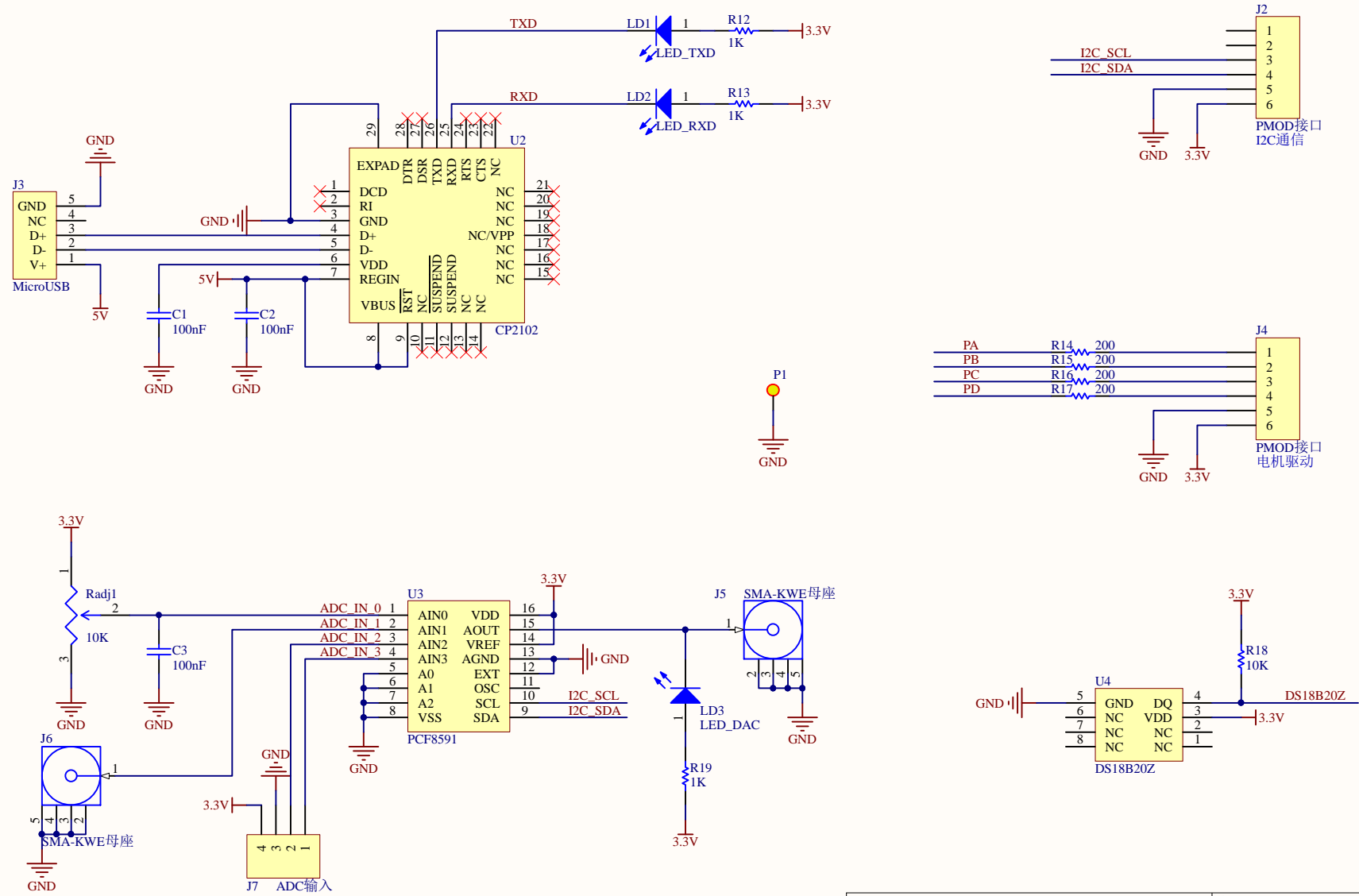


1

2

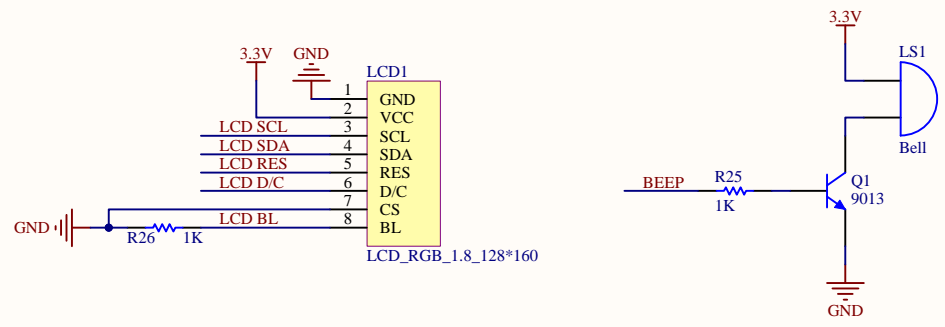
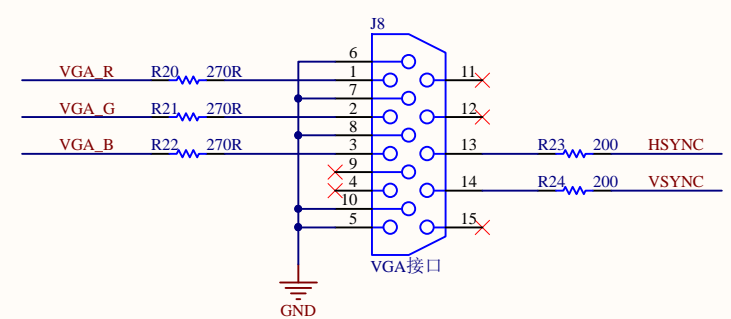
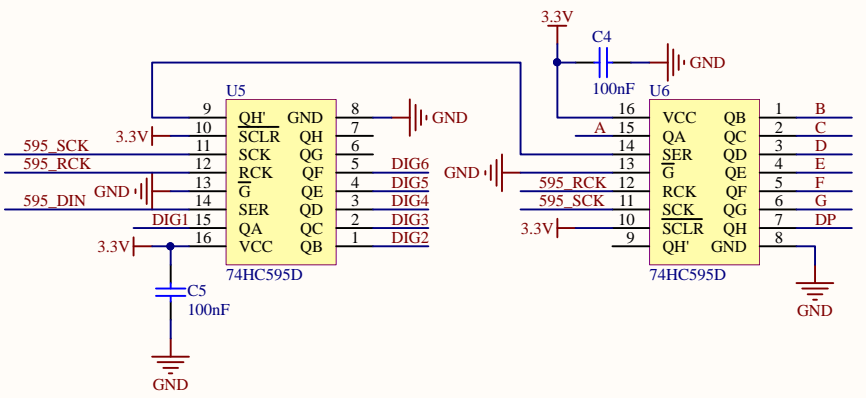
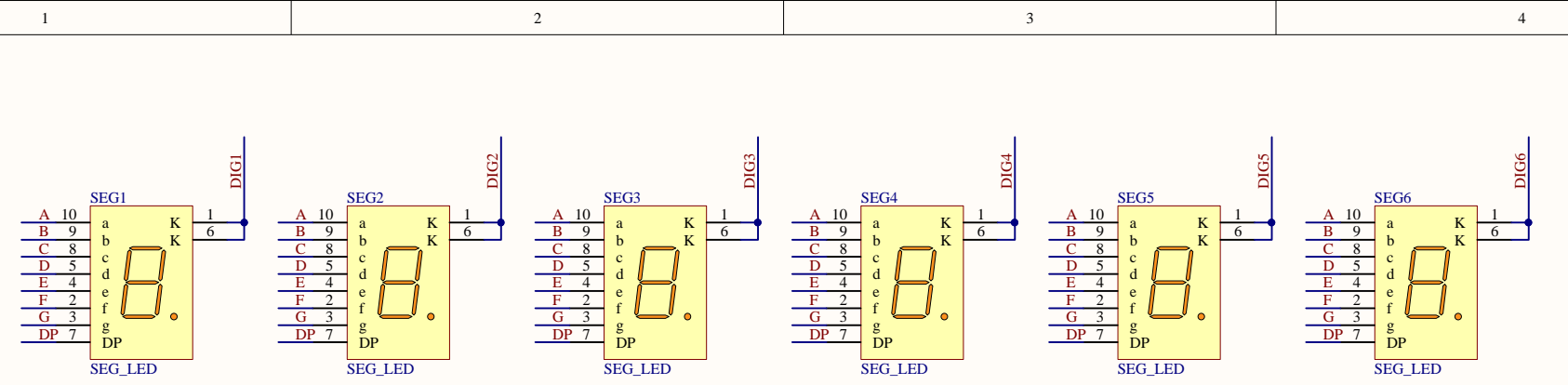
3

4



Title STEP V2.1 BaseBoard			*
Size: A4	Number:	Revision: V2.1	*
Date: 2017/5/27	Time: 10:23:40	Sheet2 of 3	*
File: F:\PCB_Project\STEP V2.1 BaseBoard_003\STEP V2.1 BaseBoard_2.SchDoc			*





Title STEP V2.1 BaseBoard			*
Size: A4	Number:	Revision: V2.1	*
Date: 2017/5/27	Time: 10:23:44	Sheet3 of 3	*
File: F:\PCB_Project\STEP V2.1 BaseBoard_003\STEP V2.1 BaseBoard_3.SchDoc			*

