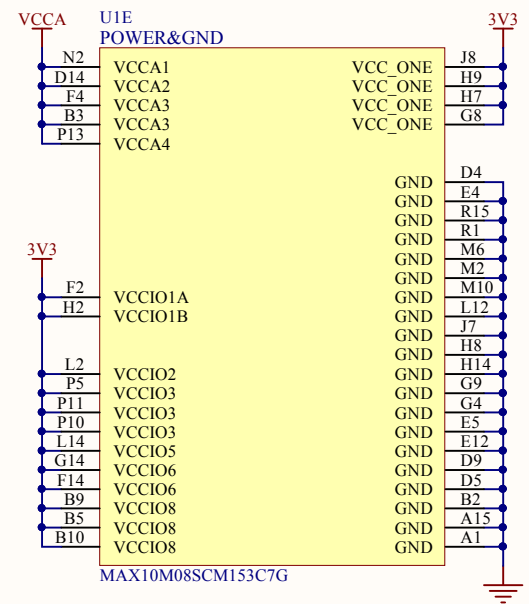
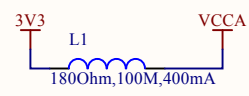
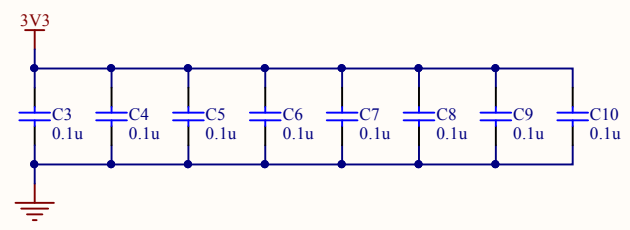
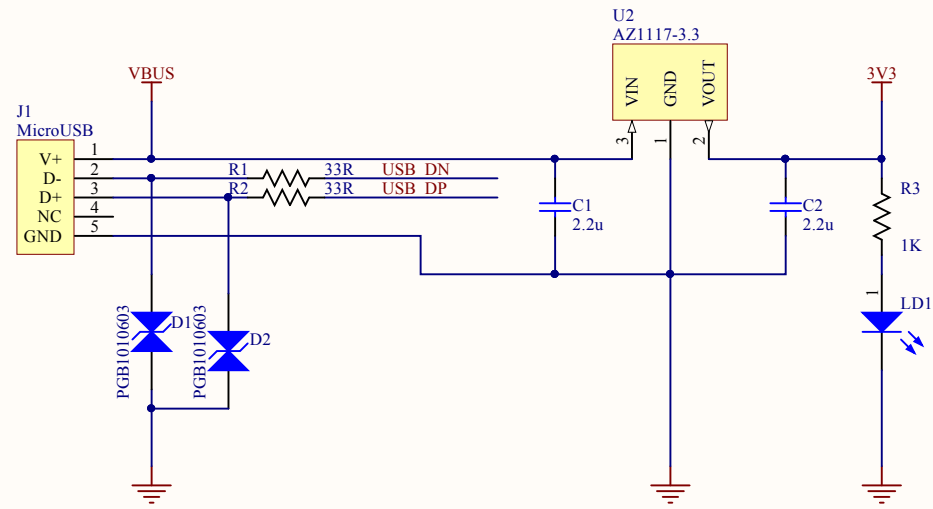


工程名称: STEP-MAX10 FPGA Board		
图纸大小: A4	版本号: V2.0	制图:
日期: 2017/5/12	页码: 第 1 共 2	审核:



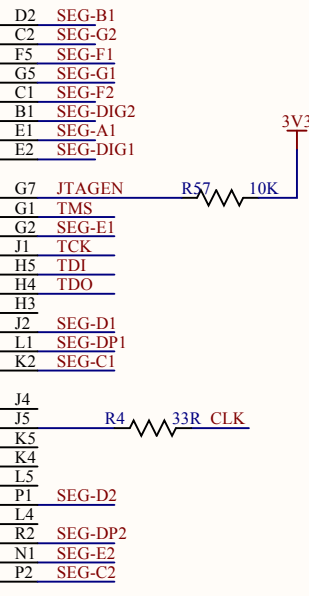
Block Diagram



工程名称: STEP-MAX10 FPGA Board		
图纸大小: A4	版本号: V2.0	制图:
日期: 2017/5/12	页码: 第 2 共 5	审核:
Power		

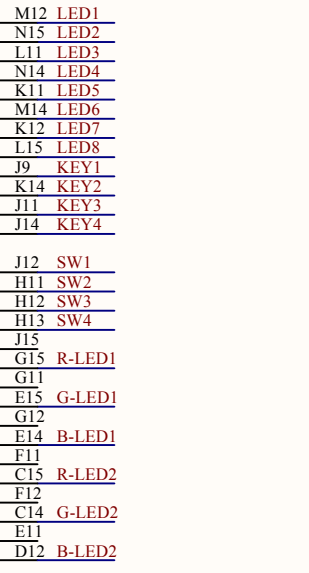


<b>U1A</b>	
<b>BANK 1A</b>	
DIFFIO_RX_L1n	D2 SEG-B1
DIFFIO_RX_L1p	C2 SEG-G2
DIFFIO_RX_L3n	F5 SEG-F1
DIFFIO_RX_L3p	G5 SEG-G1
DIFFIO_RX_L5n	C1 SEG-F2
DIFFIO_RX_L5p	B1 SEG-DIG2
DIFFIO_RX_L7n	E1 SEG-A1
DIFFIO_RX_L7p	E2 SEG-DIG1
<b>BANK 1B</b>	
JTAGEN	G7 JTAGEN
DIFFIO_RX_L11n/TMS	G1 TMS
VREFB1N0	G2 SEG-E1
DIFFIO_RX_L11p/TCK	J1 TCK
DIFFIO_RX_L12n/TDI	H5 TDI
DIFFIO_RX_L12p/TDO	H4 TDO
DIFFIO_RX_L14n	H3
DIFFIO_RX_L14p	J2 SEG-D1
DIFFIO_RX_L16n	L1 SEG-DP1
DIFFIO_RX_L16p	K2 SEG-C1
<b>BANK 2</b>	
DIFFIO_RX_L18n/CLK0n	J4
DIFFIO_RX_L18p/CLK0p	J5
DIFFIO_RX_L20n/CLK1n	K5
DIFFIO_RX_L20p/CLK1p	K4
DIFFIO_RX_L22n/DPCLK0	L5
VREFB2N0	P1 SEG-D2
DIFFIO_RX_L22p/DPCLK1	R2 SEG-DP2
DIFFIO_RX_L27n/PLL_L_CLKOUTn	N1 SEG-E2
DIFFIO_RX_L27p/PLL_L_CLKOUTp	P2 SEG-C2



MAX10M08SCM153C7G

<b>U1C</b>	
<b>BANK 5</b>	
DIFFIO_RX_R1p	M12 LED1
DIFFIO_RX_R2p	N15 LED2
DIFFIO_RX_R1n	L11 LED3
DIFFIO_RX_R2n	N14 LED4
DIFFIO_RX_R7p	K11 LED5
DIFFIO_RX_R7n	M14 LED6
VREFB5N0	K12 LED7
DIFFIO_RX_R10p	L15 LED8
DIFFIO_RX_R11p	J9 KEY1
DIFFIO_RX_R10n	K14 KEY2
DIFFIO_RX_R11n	J11 KEY3
DIFFIO_RX_R11n	J14 KEY4
<b>BANK 6</b>	
DIFFIO_RX_R14p/CLK2p	J12 SW1
DIFFIO_RX_R14n/CLK2n	H11 SW2
DIFFIO_RX_R16p/CLK3p	H12 SW3
DIFFIO_RX_R16n/CLK3n	H13 SW4
DIFFIO_RX_R18p	J15
DIFFIO_RX_R18n	G15 R-LED1
DIFFIO_RX_R26p/DPCLK3	G11
VREFB6N0	E15 G-LED1
DIFFIO_RX_R26n/DPCLK2	G12
DIFFIO_RX_R27p	E14 B-LED1
DIFFIO_RX_R28p	F11
DIFFIO_RX_R27n	C15 R-LED2
DIFFIO_RX_R28n	F12
DIFFIO_RX_R33p	C14 G-LED2
DIFFIO_RX_R33n	E11
DIFFIO_RX_R33n	D12 B-LED2



MAX10M08SCM153C7G

<b>U1B</b>	
<b>BANK 3</b>	
DIFFIO_TX_RX_B1n	M4 GPIO0
DIFFIO_RX_B2n	P3 GPIO1
DIFFIO_TX_RX_B1p	M5 GPIO2
DIFFIO_RX_B2p	R3 GPIO3
DIFFIO_TX_RX_B3n	L6 GPIO4
DIFFIO_RX_B4n	P4 GPIO5
DIFFIO_TX_RX_B3p	L7 GPIO6
DIFFIO_RX_B4p	R5 GPIO7
DIFFIO_TX_RX_B5n	P6 GPIO8
DIFFIO_RX_B6n	R7 GPIO9
DIFFIO_TX_RX_B5p	P7 GPIO10
DIFFIO_RX_B6p	P8 GPIO11
DIFFIO_TX_RX_B7n	L8
DIFFIO_RX_B8n	P9 GPIO12
DIFFIO_TX_RX_B7p	M7
DIFFIO_RX_B8p	R9 GPIO13
DIFFIO_TX_RX_B9n	M8
VREFB3N0	R11 GPIO14
DIFFIO_TX_RX_B9p	N8
DIFFIO_TX_RX_B10n	P12 GPIO15
DIFFIO_TX_RX_B10p	R14 GPIO16
DIFFIO_TX_RX_B12n	P15 GPIO17
DIFFIO_TX_RX_B12p	L9
DIFFIO_TX_RX_B14n	M9
DIFFIO_TX_RX_B14p	L10
DIFFIO_TX_RX_B16n	M11
DIFFIO_TX_RX_B16p	P14
DIFFIO_TX_RX_B16p	R13

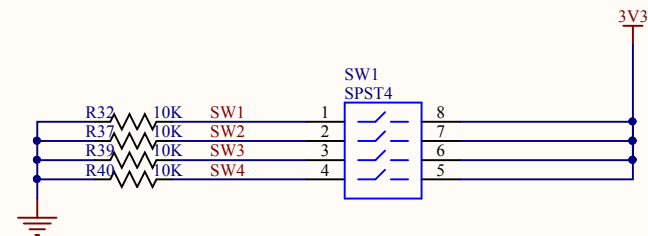
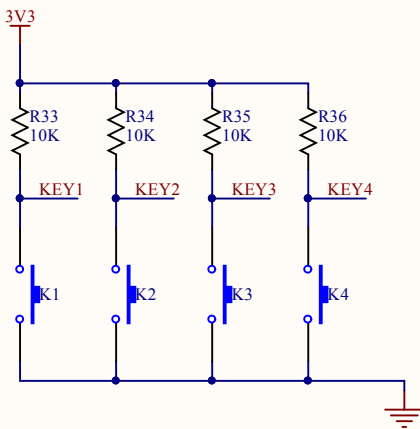
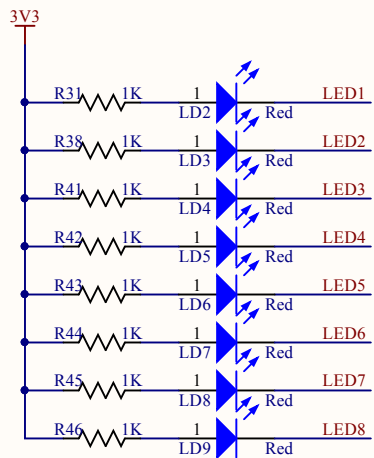
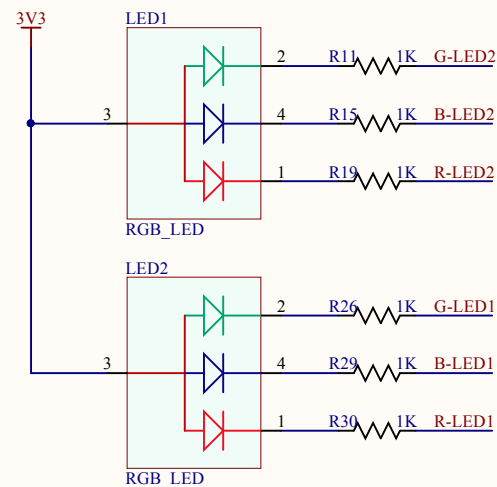
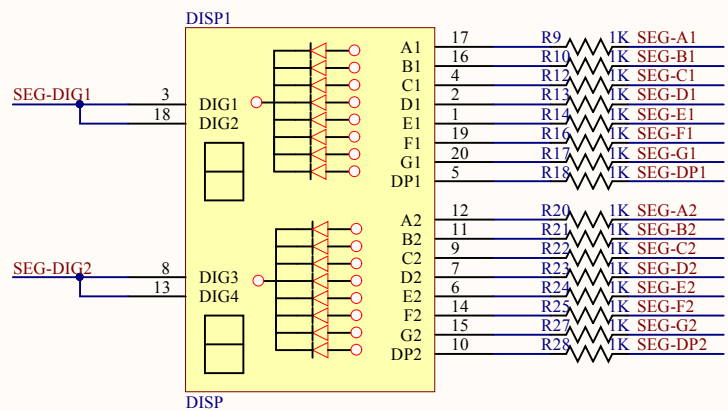
MAX10M08SCM153C7G

<b>U1D</b>	
<b>BANK 8</b>	
DIFFIO_RX_T14p	D11
DIFFIO_RX_T15p	B15 GPIO18
DIFFIO_RX_T14n	D10 GPIO26
DIFFIO_RX_T15n	B14 GPIO19
DIFFIO_RX_T16p	C8 GPIO28
DIFFIO_RX_T17p	B13 GPIO20
DIFFIO_RX_T16n/DEV_CLRn	B8 GPIO27
DIFFIO_RX_T17n	A14 GPIO21
DIFFIO_RX_T18p/DEV_OE	E10
DIFFIO_RX_T18n	E9
VREFB8N0	A13 GPIO23
CONFIG_SEL	D8 CONFIG_SEL
DIFFIO_RX_T19p	B12
nCONFIG	E8
DIFFIO_RX_T19n	B11 GPIO22
DIFFIO_RX_T20p	B7 GPIO29
DIFFIO_RX_T21p	A9 GPIO25
DIFFIO_RX_T20n	B6 GPIO32
DIFFIO_RX_T21n	A11 GPIO24
DIFFIO_RX_T22p	D7 GPIO30
DIFFIO_RX_T23p	A7 GPIO33
DIFFIO_RX_T22n/CRC_ERROR	E7 GPIO31
DIFFIO_RX_T23n	A5 GPIO34
DIFFIO_RX_T24p/nSTATUS	D6
DIFFIO_RX_T24n/CONF_DONE	B4 GPIO35
DIFFIO_RX_T26p	E6
DIFFIO_RX_T26n	A2 SEG-B2
	A3 SEG-A2

MAX10M08SCM153C7G

工程名称:	STEP-MAX10 FPGA Board				
图纸大小:	A4	版本号:	V2.0	制图:	
日期:	2017/5/12	页码:	第 3 共 5	审核:	
FPGA					





工程名称: STEP-MAX10 FPGA Board		
图纸大小: A4	版本号: V2.0	制图:
日期: 2017/5/12	页码: 第 4 共 5	审核:
LEDs,Buttons,Switchs,RGB LEDs,Segments		



